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CBCS SCHEME

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BEC602

Sixth Semester B.E./B.Tech. Degree Examination, Dec.2025/Jan.2026
VLSI Design and Testing

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Implement CMOS logic for the following compound gates. i) $F = \overline{A(B+C)+DE}$ ii) $F = \overline{(A+B+C)D}$	10	L3	CO1
	b.	Implement and explain 2 i/p multiplexes using TG and also mention advantages of TG.	10	L3	CO2
		OR			
Q.2	a.	Design flip-flop using multiplexes and inverter.	08	L3	CO2
	b.	Illustrate structural representation for 2 i/p NAND gates by adding performance parameter.	04	L3	CO2
	c.	Develop physical symbolic layout for the following. i) Inverter ii) Transmission Gate	08	L3	CO2
		Module – 2			
Q.3	a.	Explain the working principle of nMOS enhancement nmos transistor.	10	L2	CO1
	b.	Define Body Effect. Illustrate how body effect alters the V_t and give mathematical expressions.	05	L3	CO1
	c.	Discuss β_n / β_p ratio effect on transfer characteristics.	05	L3	CO1
		OR			
Q.4	a.	Draw schematic diagram of CMOS inverter and explain its D C Transfer characteristics.	12	L3	CO1
	b.	Illustrate the mechanism of Latch-up in CMOS and preventive measures.	08	L3	CO1
		Module – 3			
Q.5	a.	Explain czochoalki method for wafer processing.	06	L2	CO1
	b.	Discuss Lamda-based p-well design rules.	06	L2	CO1
	c.	Explain the Twin-tub process.	08	L3	CO1
		OR			
Q.6	a.	Describe switching characteristics of CMOS inverter with equivalent circuits to determine fall and rise time.	10	L3	CO3
	b.	Explain in brief scaling principles of MOS transistor dimensions.	10	L2	CO1
		Module – 4			
Q.7	a.	What are the advantages of Dynamic CMOS logic and explain the working of dynamic CMOS inverter with timing diagrams.	08	L3	CO4
	b.	Realize 2 inputs XOR / XNOR gate using cascode voltage switch logic.	04	L3	CO4
	c.	Implement 4 – way switch logic using Transmission gate and write layout version of CMOS logic.	08	L3	CO4

Q.			Marks	Level	CO
		OR			
Q.8	**a.**	Draw star connection for CMOS inverter layout optimization and mention its advantages.	**06**	**L3**	**CO4**
	b.	Find Euler's path for the function $Z=\overline{(A+B)+CD}$ and draw corresponding layout.	**06**	**L3**	**CO4**
	c.	Write short notes on : i) ESD Protection ii) Tristate and Bidirectional Pads.	**08**	**L2**	**CO4**
		Module – 5			
Q.9	**a.**	Implement AOI based clocked NOR SR Latch circuit with waveforms.	**10**	**L3**	**CO5**
	b.	Illustrate typical design flow of a contemporary and an ideal approach for designing system.	**10**	**L3**	**CO5**
		OR			
Q.10	**a.**	Illustrate J – K flip – flop with Nand gate JK latches with waveforms.	**10**	**L3**	**CO5**
	b.	Write short notes on : i) Adhoc Testing ii) Self Test and Build in Test.	**10**	**L2**	**CO1**

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