CBCS SCHEME

USN | | | | | | | | | |

21EC71

Seventh Semester B.E./B.Tech. Degree Examination, Dec.2025/Jan.2026
Advanced VLSI

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Discuss the channeled and channeless gate arrays. **(06 Marks)**

b. Mention the important features of PLD and explain the Essential Characteristics of FPGA. **(06 Marks)**

c. Discuss the functions of each step in the ASIC Design Flow. **(08 Marks)**

OR

2 a. Explain Dadda Multiplier [6 bit] and its advantages over Wallace. **(10 Marks)**

b. Discuss
i) Datapath Logic Cell ii) Datapath Elements iii) I/O cells **(10 Marks)**

Module-2

3 a. What is Floor Planning? Briefly explain the goals and objectives of floor planning. **(08 Marks)**

b. What is Channel Definition? Explain in brief about channel definition of an ASIC system floor planning. **(06 Marks)**

c. Explain the Mini-cut Placement method in brief. **(06 Marks)**

OR

4 a. List and goals and objectives of global routing and explain in brief about global routing methods. **(08 Marks)**

b. Explain the left edge algorithm for channel routing. **(06 Marks)**

c. Discuss the clock and power routing. **(06 Marks)**

Module-3

5 a. List the verification methodologies and explain constrained random stimulus methodology basics. **(10 Marks)**

b. Define Testbench? Explain testbench components with the help of a neat diagram. **(10 Marks)**

OR

6 a. Explain Fixed, Dynamic, Queue and associative array operations with examples. **(10 Marks)**

b. Explain the guidelines for choosing a storage type in the system varilog. **(10 Marks)**

Module-4

7 a. Write the different between Tasks and function in system verilog. **(06 Marks)**

b. Explain the routine arguments with suitable examples. **(08 Marks)**

c. Discuss time values of system verilog with examples. **(06 Marks)**

OR

8 a. Describe the communication between the testbench and DUT with suitable diagram and examples. **(10 Marks)**

b. List and explain different types of system verilog assertions. **(10 Marks)**

Module-5

9 a. What is Randomization? Explain device and environment configuration and randomization. **(10 Marks)**

b. Describe any two solution probabilities in system verilog with examples. **(10 Marks)**

OR

10 a. Define Functional Coverage. Explain coverage convergence using neat diagram. **(10 Marks)**

b. List coverage type of verification and compare code coverage and functional coverage. **(10 Marks)**

* * * * *