CBCS SCHEME

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BMT702

Seventh Semester B.E./B.Tech. Degree Examination, Dec.2025/Jan.2026
Introduction to HDL

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Explain the various types of Ports available in VHDL and verilog with example.	10	L2	CO1
	b.	Outline the process of simulation and synthesis in Hardware Description Languages.	10	L2	CO1
		OR			
Q.2	a.	List and explain the various data types in verilog with example on each type.	10	L2	CO1
	b.	Illustrate the shift and rotate operation in VHDL with example.	10	L2	CO1
		Module – 2			
Q.3	a.	Explain the signal declaration and constant declaration verilog and VHDL with an example.	10	L2	CO2
	b.	Write an expression and circuit for 2 × 2 combinational unsigned multiplier with verilog in dataflow description.	10	L3	CO2
		OR			
Q.4	a.	Write an expression, truth table and circuit for Ripple carry adder in VHDL dataflow description.	10	L3	CO2
	b.	Write 2 × 4 decoder in VHDL and verilog using dataflow description.	10	L2	CO2
		Module – 3			
Q.5	a.	List and explain the highlight of behavioral description with an example program.	10	L2	CO3
	b.	Illustrate the signal assignment and variable assignment with an example and timing diagram.	10	L2	CO3
		OR			
Q.6	a.	Write a program to calculate the factorial of positive integer using behavioral description in verilog.	10	L2	CO3
	b.	Explain the following with syntax and example i) repeat ii) forever iii) wait for	10	L2	CO3

		Module – 4			
Q.7	a.	List the binding methods and explain a binding technique used in verilog with an example.	10	L2	CO4
	b.	Write a verilog program in structural description for 2 × 1 multiplexer.	10	L2	CO4
		OR			
Q.8	a.	Explain the following binding methods in VHDL with example. i) Library and component ii) Library and module	10	L2	CO4
	b.	Write a program for SR latch with NOR gates in verilog using structural description.	10	L2	CO4
		Module – 5			
Q.9	a.	Describe the steps involved in design of Finite State Machine (FSM) with a suitable example.	10	L2	CO5
	b.	Explain the following with syntax and example. i) Generic ii) Parameter.	10	L2	CO5
		OR			
Q.10	a.	Design a 3-bit synchronous even counter using master slave JK-FF, Sketch the FSM with a verilog code.	10	L2	CO5
	b.	Write a structural description of an n-bit asynchronous down counter using generate statement in VHDL.	10	L2	CO5

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