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10ELN15/25

First/Second Semester B.E. Degree Examination, Dec.2017/Jan.2018
Basic Electronics

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Choose the correct answers for the following : **(04 Marks)**

i) A diode has _____ terminals and _____ junctions
A) 2, 2 B) 1, 1
C) 2, 1 D) 1, 2

ii) The line connecting I_F and V_F on the diode forward characteristics is called as ____line
A) Power B) Forward
C) AC load D) DC load

iii) The intersection of the diode forward characteristics and the DC load line is called as
A) P Point B) Q Point
C) R Point D) S Point

iv) A filter connected to a rectifier output removes
A) Ripple B) Attenuation
C) Noise D) Unwanted frequency.

b. Draw a Labelled circuit diagram of a half wave rectifier with C filter and explain the associate waveforms. **(08 Marks)**

c. Design Zener diode voltage regulator to meet the following specifications :

Unregulated DC input voltage V_i : 8V to 12V
Regulated DC output voltage V_0 : 5V
Minimum Zener current I_{Zmin} : 5mA
Maximum Zener current I_{Zmax} : 80mA
Load current I_L : 0 t 20mA. **(08 Marks)**

2 a. Choose the correct answers for the following : **(04 Marks)**

i) β_{DC} of a transistor is given by
A) $\frac{I_B}{I_C}$ B) $\frac{I_C}{I_E}$
C) $\frac{I_C}{I_B}$ D) $\frac{I_E}{I_C}$

ii) The common–Emitter output characteristics waveform is plotted as ____ Vs _____
A) V_{CE}, I_C B) V_{BE}, I_C
C) V_{CE}, I_E D) V_{BE}, I_E

iii) The DC loadline drawn on the CE output characteristics has a slope of
A) 1/RC B) –RC
C) R_C D) $-1/R_C$

iv) For the normal operation of a transistor, Base–Emitter junction is _____ biased and collector–base junction is _____ biased
A) FB, FB B) FB, RB
C) RB, FB D) RB, RB

b. Draw the circuit diagram of a PNP transistor in common –base configuration and explain its input and output characteristics. **(08 Marks)**

c. Find α_{DC}, I_B and β_{DC} for a transistor with I_C = 2.5mA and I_E = 2.55mA. **(04 Marks)**

d. Explain the significance of active, cutoff and saturation regions in a transistor. **(04 Marks)**

3 a. Choose the correct answers for the following : **(04 Marks)**

i) Biasing a transistor means

A) Applying heat B) Discharging

C) Displacing D) Applying Voltages

ii) A transistor in CE configuration having collector current zero has V_{CE} as

A) $\frac{V_{CC}}{R_C + R_E}$ B) $\frac{V_{CC}}{R_C}$

C) V_{CC} D) $\frac{V_{CC}}{R_E}$

iii) The biasing circuit which gives most stable operating point is

A) Base bias B) Voltage –divider

C) Collector–base D) Emitter

iv) The stability factor $S = 1 + \beta_{DC}$ applies to _____ biasing

A) Base B) Voltage-divider

C) Collector–base D) Emitter.

b. Sketch the circuit of voltage divider bias and discuss its approximate analysis. **(08 Marks)**

c. A collector–to–base bias circuit shown in Fig.Q3(c) has $V_{CC} = 15V$, $R_C = 1.8k\Omega$, $R_B = 39k\Omega$ $\beta_{DC} = 50$ and $V_{BE} = 0.7V$. Determine the I_C and V_{CE} levels. Draw the DC load line and locate the Q point. **(08 Marks)**

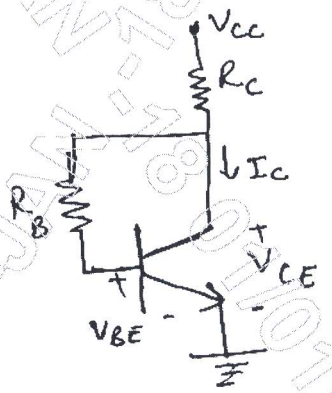

Fig.Q3(c)

4 a. Choose the correct answers for the following : **(04 Marks)**

i) An SCR is a _____ with a gate

A) Oscillator B) Rectifier

C) Regulator D) Clipper

ii) Over voltage protection circuit in an SCR is called as

A) Hen bar B) Bird bar

C) Sparrow bar D) Craw bar

iii) An UJT has _____ bases

A) Two B) Three

C) Zero D) One

iv) Pinch-off voltage is normally associated with

A) Diode B) UJT

C) JFET D) SCR.

b. Draw a circuit diagram for UJT and sketch and explain the V-I characteristics mentioning different regions. **(08 Marks)**

c. Explain the structure and operation of an n-channel JFET. **(04 Marks)**

d. Draw the forward characteristics of an SCR with suitable labeling. Describe the characteristics curves. **(04 Marks)**

PART – B

5 a. Choose the correct answers for the following : **(04 Marks)**

i) For a 2-stage amplifier with gain A_{V1} and A_{V2} for Stage-1 and Stage-2, the overall gain A_V is

A) $A_{V1} \times A_{V2}$ B) $A_{V1} + A_{V2}$
C) $A_{V1} - A_{V2}$ D) A_{V1}/A_{V2}

ii) A oscillator requires input as

A) DC input B) No input
C) AC input D) Any input

iii) Hartley and Colpitts oscillator use _____ circuit to generate oscillations

A) Bucket B) Tap
C) Drum D) Tank

iv) The frequency of oscillation for a colpitts oscillator is given by $1/\left(2\pi\sqrt{LC}\right)$ where C is

A) $C_1\ C_2$ B) $C_1 + C_2$

C) $\frac{C_1\ C_2}{C_1 + C_2}$ D) $\frac{C_1 + C_2}{C_1\ C_2}$.

b. Draw the circuit diagram of a single stage common emitter RC coupled amplifier and explain various component in the circuit, mentioning the input and output waveforms. **(08 Marks)**

c. Find the values of L and C for a colpitts oscillator whose frequency of oscillation is 40KHz. Assume L = 10mH, $C_1 = C_2$. Find C_1 and C_2. **(04 Marks)**

d. State Barkhasen criteria used for sustained Oscillations and mention any two reasons for using –ve feedback. **(04 Marks)**

6 a. Choose the correct answers for the following : **(04 Marks)**

i) An Op-Amp has _____ input terminals

A) One B) Two
C) Three D) Four

ii) An ideal Op-Amp has input resistance and output resistance as

A) ∞ and O B) O and ∞
C) O and O D) ∞ and ∞

iii) Deflection system in a CR_0 consists of _____

A) Horizontal B) Vertical
C) Diagonal D) horizontal and Vertical

iv) In an Op-Amp inverting amplifier $R_\ell = 1k\Omega$, $R_f = 10\ k\Omega$. The output voltage is _____ if the input voltage is 2V

A) –10V B) 12V
C) –20V D) 8V.

b. Design an inverting adder circuit using Op-Amp to obtain an output voltage given by $V_0 = 2[0.1V_1 + 0.5V_2 + 2.0V_3]$ where V_1, V_2, V_3 are the input voltages. Assume $R_f = 10k\Omega$. **(06 Marks)**

c. With a neat diagram explain how an Op-Amp can be used as a differentiator. **(06 Marks)**

d. List out any Four ideal characteristics of Op-Amp. **(04 Marks)**

7 a. Choose the correct answers for the following : **(04 Marks)**

i) In a superheterodyne receiver the output of the mixer is always _____

A) 455 KHz B) 1055 KHz
C) 955 KHz D) 544 KHz

ii) 2's complement of 10101 is

A) 00011 B) 01010
C) 01011 D) 10100

iii) $(001001101)_2 = (\quad\_\_\_\_\quad)_{16}$

A) $(113)_{16}$ B) $(261)_{16}$
C) $(4D0)_{16}$ D) $(04D)_{16}$

iv) The maximum power in an AM system is _____

A) P_C B) $1.5P_C$
C) $0.5P_C$ D) $0.99P_C$

b. Draw the block diagram of a superheterodyne AM receiver. Explain the function of each block mentioning the waveforms at the outputs of each block. **(08 Marks)**

c. Convert $(110101)_2 = (\quad)_{10} = (\quad)_{16} = (\quad)_8 = (\quad)_{BCD}$. **(04 Marks)**

d. Simplify the following expression and implement using N and gates only :

$F = ZY + \overline{Z} + XYZ$. **(04 Marks)**

8 a. Choose the correct answers for the following : **(04 Marks)**

i) When Demorgan's theorem applied to $\overline{A \cdot B}$, we get _____

A) $A \cdot B$ B) $\overline{A} + \overline{B}$
C) A D) B

ii) $Y = AB + \overline{A}\,\overline{B}$ is a Boolean expression for _____ gate

A) OR B) NOR
C) E XOR D) E XNOR

iii) Universal gates are

A) AND, NAND B) OR, NOR
C) NOR, NAND D) AND, OR

iv) $A + \overline{A}B =$

A) A + B B) B
C) A D) $\overline{A}$ B

b. With a neat diagram, explain the working principle of a parallel binary adder. Give a numerical example. **(08 Marks)**

c. Realize $Y = \overline{A}\,B + A\,\overline{B}$ using NAND gates only after simplification. **(04 Marks)**

d. Realize $Y = \overline{A}\,B + A\,\overline{B}$ using NOR gates only after simplification. **(04 Marks)**

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