CBCS SCHEME

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17EE34

Third Semester B.E. Degree Examination, Dec.2018/Jan.2019
Analog Electronic Circuits

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Draw a double ended clipper circuit and explain its working principle with transfer characteristics. **(07 Marks)**

b. Draw and explain the working of clamper circuit which clamps the positive peak of a signal to zero. **(07 Marks)**

c. With suitable graph, explain the significance of operating point. **(06 Marks)**

OR

2 a. Derive the expression for stability factor for fixed bias circuit, with respect to I_{co}, V_{BE} and β. **(07 Marks)**

b. A voltage divider biased circuit has $R_1 = 39k\Omega$, $R_2 = 82k\Omega$, $R_c = 3.3k\Omega$, $R_E = 1k\Omega$ and $V_{CC} = 18V$. The Silicon transistor used has $\beta = 120$. Find Q-point and stability factor. **(08 Marks)**

c. Calculate the Q point values (I_c and V_{CE}) for the circuit given in Fig Q2(c). **(05 Marks)**

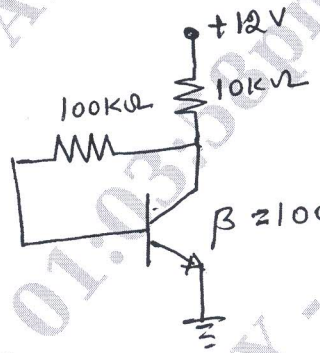

Fig Q2(c)

Module-2

3 a. State and prove Millers theorem. **(08 Marks)**

b. Starting from fundamentals define h-parameters and obtain an h-parameter equivalent circuit of common emitter configuration. **(08 Marks)**

c. Compare the characteristics of CB, CE and CC configurations. **(04 Marks)**

OR

4 a. Derive an expression for input impedance volt gain, current gain and output impedance for an emitter follower circuit using h-parametesr model for the transistor. **(08 Marks)**

b. For the transistor connected in CE configuration, determine A_v, A_I, R_I and R_o using complete hybrid equivalent model.
Given $R_L = R_s = 1k\Omega$, $h_{ie} = 1k\Omega$, $h_{re} = 2\times10^{-4}$, $h_{fe} = 100$ and $h_{oe} = 20\mu A/V$ **(08 Marks)**

c. A transistor in CE mode has h-parameters
$h_{ie} = 1.1k\Omega$, $h_{re} = 2\times10^{-4}$, $h_{fe} = 100$ and $h_{oe} = 25\mu A/V$. Determine the equivalent CB parameters. **(04 Marks)**

Module-3

5 a. Draw the circuit of Darlington emitter follower. Derive the expression for current gain using its ac equivalent circuit. **(08 Marks)**

b. What are the advantages of negative feedback in amplifiers? Explain briefly. **(06 Marks)**

c. For the voltage series feedback amplifier, derive an expression for output impedance. **(06 Marks)**

OR

6 a. Explain the need of cascading amplifier. Draw and explain the block diagram of two stage cascade amplifier. **(08 Marks)**

b. A given amplifier arrangement has the following voltage gains $A_{V_1} = 10$ $A_{V_2} = 20$ and $A_{V_3} = 40$. Calculate the overall voltage gain and determine the total voltage gain in dBs. **(06 Marks)**

c. An amplifier with negative feedback has a voltage gain of 120. It is found that without feedback an input signal of 60mV is required to produce a particular output, whereas with feedback the input signal must be 0.5V to get the same output. Find voltage gain (A_V) and β of the amplifier. **(06 Marks)**

Module-4

7 a. Derive an expression for frequency of oscillations in Wien bridge' oscillator. **(08 Marks)**

b. Explain the operation of class B push pull amplifier. Prove that the maximum efficiency of class B configuration is 78.5%. **(08 Marks)**

c. A crystal has following parameters. L = 0.3344H, C = 0.065pF, C_m = 1pF and R = 5.5kΩ. Calculate: i) Series resonance frequency ii) Parallel resonance frequency. **(04 Marks)**

OR

8 a. Explain the operation of class A transformer coupled power amplifier and prove that the maximum efficiency is 50%. **(08 Marks)**

b. A class B push pull amplifier operating with V_{CC} = 25V provides a 22V peak signal to 8Ω load. Calculate circuit efficiency and power dissipated per transistor. **(06 Marks)**

c. Explain the principle of operation of oscillator and the effect of loop gain (Aβ) on the output of oscillator. **(06 Marks)**

Module-5

9 a. With the help of neat diagram, explain the working and characteristics of N-channel JFET. **(08 Marks)**

b. Determine Z_I, Zo and A_v for JFET common source amplifier with fixed bais configuration using AC equivalent small signal model. **(08 Marks)**

c. Write down the differences between BJT and JFET. **(04 Marks)**

OR

10 a. With the help of neat diagrams, explain the construction, working and characteristics of N-channel depletion type MOSFET. **(10 Marks)**

b. Write down the differences between MOSFET and JFET. **(04 Marks)**

c. For the circuit given in the Fig Q10(c), determine: i) Input impedance ii) Output impedance and iii) voltage gain. **(06 Marks)**

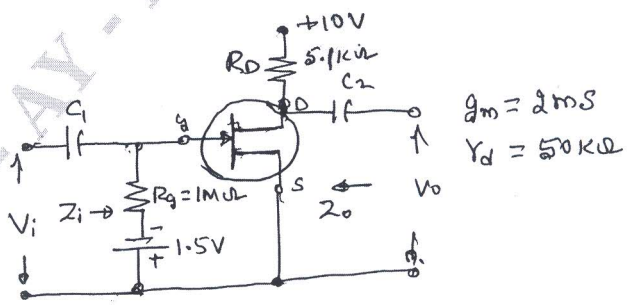

Fig Q10(c)

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