

# CBCS Scheme

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15EC33

Third Semester B.E. Degree Examination, June/July 2018

## Digital Electronics

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

### Module-1

- 1 a. Given,  $F = A(B + C) + D$ , obtain : i) minimal SOP ii) minimal POS iii) canonical SOP  
iv) canonical POS. (08 Marks)
- b. Realize a circuit for Ex-NOR using only four NOR gates. (02 Marks)
- c. Simplify the function using K-map. :  
 $Y = f(a, b, c, d) = \sum_m(0,1,2,3,5,6,8,10,15)$ .  
Write the simplified SOP expression. (06 Marks)

OR

- 2 a. Simplify the following function using Quine – McClusky method :  
 $P = f(a, b, c, d) = \sum_m(0, 2, 3, 5, 8, 10, 11, 13)$ . (06 Marks)
- b. Reduce the following Boolean function using K-map and realize the simplified expression using NOR gates.  
 $T = f(a, b, c, d) = \sum_m(0, 2, 3, 5, 6, 7, 8, 9) + \sum_d(10, 11, 12, 13, 14, 15)$ . (06 Marks)
- c. Prove that,  $ABC + \overline{A}BC + A\overline{B}C + \overline{A}\overline{B}C = AB + BC + CA$  (04 Marks)

### Module-2

- 3 a. Design a binary full subtractor using logic gates. Write a truth table Implement the logic circuit using basic gates. (06 Marks)
- b. Define magnitude comparator. Design a two bit binary comparator and implement with suitable logic gates. (10 Marks)

OR

- 4 a. Implement full adder using 4 : 1 multiplexer (MUX). (08 Marks)
- b. With a neat logic diagram, explain carry look ahead adder. (08 Marks)

### Module-3

- 5 a. Obtain the characteristic equation for D and T flip-flop. (04 Marks)
- b. Explain the working of a master–slave SR flip-flop with the help of a logic diagram, function table, logic symbol and timing diagram. (08 Marks)
- c. Differentiate sequential logic circuit and combinational logic circuit. (04 Marks)

OR

- 6 a. Explain the working of master slave JK flip-flops with functional table and timing diagram. Show how race around condition is over come. (08 Marks)
- b. Discuss the difference between a flip-flop and latch. (04 Marks)
- c. Derive the characteristic equations of SR and JK flip-flops. (04 Marks)

**Module-4**

- 7 a. Design a synchronous mod-5 counter using JK flip-flops and implement it. (08 Marks)  
b. Design/synchronous mod-6 counter using D flip-flop to generate the count sequence, (0, 2, 3, 6, 5, 1, 0). (08 Marks)

**OR**

- 8 a. Design divide by 6 synchronous counter using T – flip-flops. Write state table and reduce the expression using K-map. (06 Marks)  
b. Compare synchronous and asynchronous counters. (04 Marks)  
c. Design mod-6 ripple counter using T flip-flops. (06 Marks)

**Module-5**

- 9 a. Design a Moore type sequence detector to detect a serial input sequence of 101. (08 Marks)  
b. Design a synchronous counter using JK – flip-flops to count the sequence 0, 1, 2, 4, 5, 6, 0, 1, 2. Use state diagram and state table. (08 Marks)

**OR**

- 10 a. Explain the Mealy model and Moore model of a clocked synchronous sequential network. (08 Marks)  
b. Design a Mealy type sequence detector to detect a serial input sequence of 101. (08 Marks)

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