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10ES32

Third Semester B.E. Degree Examination, Dec.2018/Jan.2019
Analog Electronic Circuits

Time: 3 hrs. Max. Marks:100

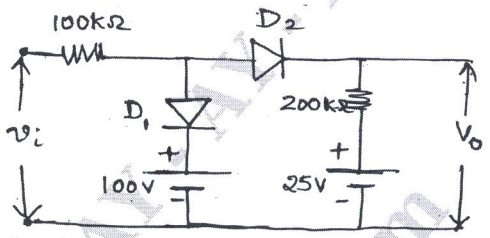
Note: ***Answer any FIVE full questions, selecting at least TWO full questions from each part.***

PART – A

1 a. Derive the expression for dynamic resistance of the diode. Determine the dynamic resistance of the diode when the diode current is 2mA. **(06 Marks)**

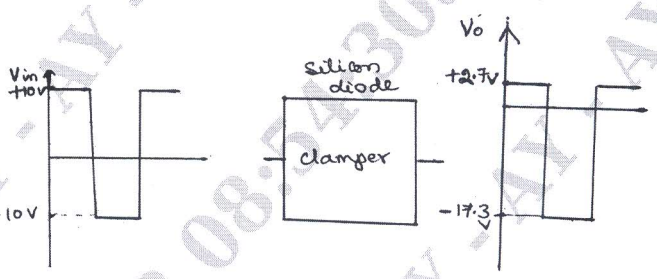
b. The input voltage to the clipper circuit shown below in Fig.Q.1(b) varies linearly from 0 to 150 volts. Draw the transfer characteristics, indicate the slope and status of diode at each level. **(08 Marks)**

Fig.Q.1(b)



c. Design the clamper circuit for the input-output waveform shown in Fig.Q.1(c) using silicon diode. **(06 Marks)**

Fig.Q.1(c)



2 a. Derive the expression for the stability factor of the Emitter Bias circuit with respect to I_{CO} and V_{BE}. **(06 Marks)**

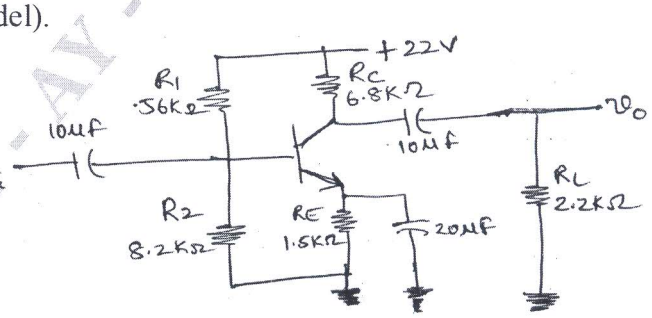
b. How do you find the operating point of fixed Bias circuit? **(04 Marks)**

c. Design a voltage divider Bias circuit using a silicon transistor with B = 100 when V_{CC} = 12V, V_{CE} = 6V, I_C = 1mA, S = 20 and V_E = 1V. **(10 Marks)**

3 a. Derive the expression for the current gain, input impedance, voltage gain and output impedance for CE configuration using hybrid model. **(10 Marks)**

b. Find r_e, A_I, Z_I, A_V and Z_O for the amplifier circuit shown in Fig.Q.3(b) with B = 120 and r_o = 40KΩ (use r_e model). **(10 Marks)**

Fig.Q.3(b)



4 a. Determine the lower cut off frequencies f_{Li} and f_{Lo} for the circuit diagram shown in Fig.Q.3(b) with $R_S = 1K\Omega$. **(06 Marks)**

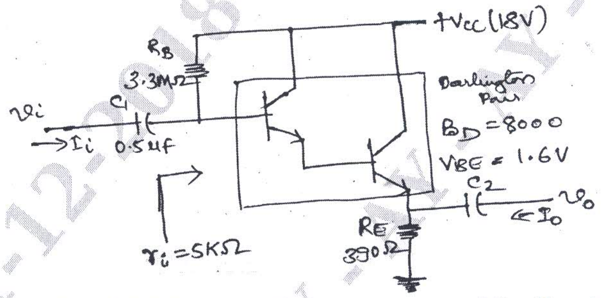
b. What is miller effect? Explain. **(06 Marks)**

c. Determine the upper cut off frequencies f_{Hi} and f_{Ho} also f_B and f_T for the circuit shown in Fig.Q.3(b) given $C_\pi (C_{be}) = 36$ pF, $C_u (C_{bc}) = 4$pF $C_{ce} = 1$pF $C_{wo} = 8$pF $C_{wi} = 6$pF. **(08 Marks)**

PART – B

5 a. Calculate Z_i, A_i, A_v and Z_o of the Darlington pair shown in Fig.Q.5(a). Derive the formulas used. **(08 Marks)**

Fig.Q.5(a)



b. What are the merits of feedback? What are different types of feedback connections? **(06 Marks)**

c. Derive the expression for A_f, Z_{if} and Z_{of} for voltage shunt feedback circuit. **(06 Marks)**

6 a. Explain the classification of power amplifiers. **(04 Marks)**

b. Explain how the efficiency of class A amplifiers increases from 25% to 50%. When we use transformer coupling. **(08 Marks)**

c. A class B power amplifier is delivering an output voltage of 10 volts peak to a 8Ω load. If the dc power supply is 30 volts, calculate:
   i) DC power input
   ii) AC power delivered to the load
   iii) Conversion efficiency
   iv) Power dissipated in the collector of each transistor. **(08 Marks)**

7 a. Derive the expression for frequency of oscillation of transistor phase shift oscillator. What is the value of current gain required for the loop gain to be greater than unity? **(10 Marks)**

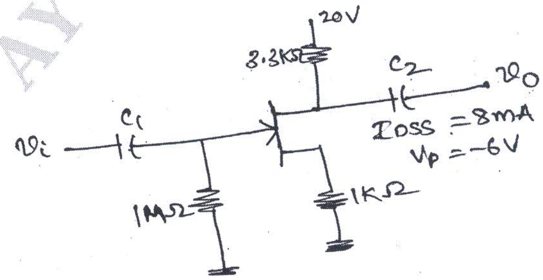
b. With a neat circuit diagram, explain the working of the Hartley oscillator. Calculate the frequency of oscillation for C = 250 PF, $L_1 = 1.5$ mH, $L_2 = 1.5$ mH and M = 0.5 mH. **(10 Marks)**

8 a. Write the ac equivalent model of JFET? Explain. **(04 Marks)**

b. Derive the expression for Z_i, Z_o, and A_v for common source JFET amplifier with fixed bias. **(06 Marks)**

c. For the JFET amplifier shown in Fig.Q.8(c), the operating point is $V_{GSQ} = -2.6$V and $I_{DQ} = 8$mA with $I_{DSS} = 8$mA and $V_P = -6$V. The value of Y_{OS} is given as 20μS determine:
i) g_m ii) r_d iii) z_i iv) calculate z_o with and without r_d v) calculate A_v with and without r_d. **(10 Marks)**

Fig.Q.8(c)



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