CBCS SCHEME

USN | | | | | | | | | | |

15EC63

Sixth Semester B.E. Degree Examination, Dec.2018/Jan. 2019
VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Mention any two differences between CMOS and Bipolar technology. **(02 Marks)**

b. Write all the mask steps of p-well process. **(06 Marks)**

c. With neat diagrams, explain the cut off, linear and saturation regions formation in MOSFET with different values of V_{gs} and V_{ds}. **(08 Marks)**

OR

2 a. Explain body effect as non ideal IV effects of MOSFET. **(03 Marks)**

b. Explain Noise margin, with respect to CMOS inverter. **(05 Marks)**

c. Explain the steps of n-MOS fabrication with neat diagram. **(08 Marks)**

Module-2

3 a. With a neat diagram, explain λ - rules for buried and butting contact and show thE cross sectional view of same. (white any one structure burreid contact). **(08 Marks)**

b. Estimate the rise time and fall time of a CMOS inverter and summarise the result. **(08 Marks)**

OR

4 a. Define sheet resistance, with equation. **(02 Marks)**

b. Calculate the area capacitance of the layer below [Refer Fig.Q4(b)] :

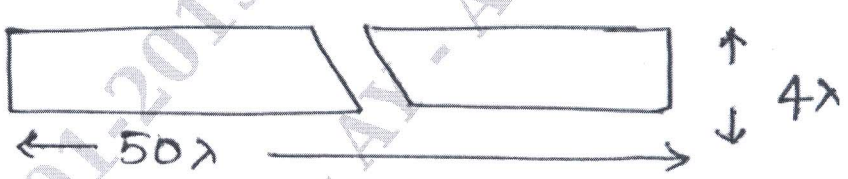

Fig.Q4(b)

i) If the layer is metal – 1 and relative capacitance value is 0.075 $\square C_g$

ii) if the layer is polysilicon and relative capacitance value is $0.1\square C_g$. **(06 Marks)**

c. Write the schematic and stick diagram for Boolean expression $y = \overline{(a + bc)}$.(implement using CMOS logic). **(08 Marks)**

Module-3

5 a. Design a 4bit, 4 × 4 barrel shifter. Write the nMOS implementation and strategy for the same. **(08 Marks)**

b. Explain carry select adder with neat block diagram. **(08 Marks)**

OR

6 a. Define regularity. **(02 Marks)**

b. Derive the scaling factor for the device parameter :

i) Parasitic capacitance

ii) Channel resistance

iii) Gate delay. **(06 Marks)**

c. Implement the ALU functions like EX-OR, EX-NOR AND and OR operations with an adder. Write the block diagram of 4-bit ALU using adder element. **(08 Marks)**

Module-4

7 a. Explain the following logics :

i) Clocked CMOS logic

ii) n-p CMOS logic. **(08 Marks)**

b. Explain parity generator, with the nMOS implementation of parity generator with stick diagram. **(08 Marks)**

OR

8 a. Explain Pseudo-nMOS logic. Find Z_{pu}/Z_{pd} when $V_{inr} = 0.5V_{DD}$, $V_{tn} = \left|V_{t_p}\right| = 0.2V_{DD}$, $V_{DD} = 5V$ and $\mu_n = 2.5\mu p$. **(08 Marks)**

b. Explain the 4-way data selector (multiplexer) with Boolean equation and nMOS based stick diagram. **(08 Marks)**

Module-5

9 a. Write the system timing considerations. **(08 Marks)**

b. Explain logic verification principle. **(08 Marks)**

OR

10 a. Explain three transistor dynamic RAM with neat circuit and stick diagram. **(06 Marks)**

b. What are design manufacturability. **(10 Marks)**

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