CBCS SCHEME

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15EC663

Sixth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Digital System Design using Verilog

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Explain with illustration, a simple design methodology followed in IC industries. **(08 Marks)**

b. Explain the following constraints imposed in real world circuits :
i) Noise margin ii) propagation delay. **(03 Marks)**

c. Develop a verilog model for a 7–segment decoder, include an additional input, blank, that overrides the BCD i/p and causes all segments not to be lit. **(05 Marks)**

OR

2 a. Develop a verilog module of a debouncer for a push button switch that uses a debounce interval of 10ns. Assume the system clock frequency is 50 MHz. **(06 Marks)**

b. Design and develop a circuit and verilog module for modulo 10 counters. **(06 Marks)**

c. What is the distinction between a Moore and Mealy finite state machine? **(04 Marks)**

Module-2

3 a. Write a symbol for basic memory component and explain its parts. **(06 Marks)**

b. Explain about the multiport memories. **(06 Marks)**

c. Compute the 12-bit ECC word corresponding to the 8-bit data word "0110001". **(04 Marks)**

OR

4 a. Design a 64 K × 16 bit composite memory using 16K × 8 bit component. **(08 Marks)**

b. What is the difference between asynchronous static RAM and synchronous static RAM? **(06 Marks)**

c. Using a Hamming code, how many check bits are required for single error correction and double error detection for 4-bit data word? **(02 Marks)**

Module-3

5 a. Design a priority encoder that has 16 inputs, i[0 : 15]; a 4-bit encoded output, z[3 : 0] and a valid output ie. '1' when any input is '1'. Input i[0] has the highest priority and i[15] is the lowest priority. **(08 Marks)**

b. Explain the concept of differential signaling. How does differential signaling improve noise immunity? **(08 Marks)**

OR

6 a. What are the purpose of logic blocks and I/O blocks in FPGA? **(06 Marks)**

b. Explain different types of PCB design. **(03 Marks)**

c. Explain with a neat diagram of the internal organization of a CPLD. **(07 Marks)**

Module-4

7 a. What are the purpose of following in an I/O controller : i) input register ii) output register iii) control register iv) status register. **(06 Marks)**

b. Explain neatly the designing a R-string DAC. **(05 Marks)**

c. Explain about tristate buses and weak drive. **(05 Marks)**

OR

8 a. Design and develop a verilog code for an input controller that has 8-bit binary-coded input from a sensor. The value can be read from an 8-bit input register. The controller should interrupt the embedded Gumnut. When input value changes the controller is the only interrupt in the system. **(08 Marks)**

b. What are the serial input standards? Briefly explain each. **(08 Marks)**

Module-5

9 a. Explain the design flow of hardware/software co-design. **(10 Marks)**

b. Briefly describe techniques used in power optimization. **(06 Marks)**

OR

10 a. What is the distinction between logical partition and physical partition? **(08 Marks)**

b. Explain Built-In–Self–Test (BIST) techniques. **(08 Marks)**

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