CBCS Scheme

USN | | | | | | | | | | |

15MT35

Third Semester B.E. Degree Examination, Dec.2017/Jan.2018
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. With a neat circuit diagram analyze the operation of full wave rectifier with C filter and also evaluate the expression for ripple factor for full wave rectifier with 'C' filter. **(08 Marks)**

b. A zener diode regulator has the following circuit parameters V_I = 10 V, V_Z = 5V, $R_Z = 100\ \Omega$, $R_D = 500\ \Omega$. Evaluate:
i) Output resistance
ii) Percentage change in V_L for 25% change in V_I
iii) Power dissipation in regulator circuit
iv) Voltage regulation assuming $R_L = 0.5\ K\Omega$. **(08 Marks)**

OR

2 a. Explain the following terms with respect to PN junction model:
i) DC restorer circuit
ii) Reverse recovery time
iii) Transition capacitance **(09 Marks)**

b. Create a double ended clipper model to clip at two independent levels 3V and 2V from 10V(p-p) input voltage. Also draw the transfer characteristics. **(07 Marks)**

Module-2

3 a. Evaluate the expression for gain of a first order Butterworth low pass filter. Plot the frequency response. Also mention the design steps. **(10 Marks)**

b. Evaluate the low cutoff frequency for the second order high pass Butterworth filter. Given $C_2 = C_3 = 0.0047\mu F$, $R_2 = R_3 = 33\ K\Omega$ and also draw the circuit diagram. **(06 Marks)**

OR

4 a. With a neat circuit analyze the working of RC phase shift oscillator. Using OPAMP design a RC phase shift oscillator to have F_0 = 2 kHz. **(10 Marks)**

b. Design a first order low pass filter of cut off frequency 1 kHz with a pass band gain of 2 and using frequency sealing technique convert 1 kHz cut off frequency to 1.6 kHz. **(06 Marks)**

Module-3

5 a. Understand and analyze the working of a astable multivibrator with a neat circuit and necessary waveforms. **(10 Marks)**

b. Analyze monostable multivibrator as a divide by 2 network for the frequency of input trigger signal 2 kHz. If the value of c = 0.01 μF. What should be the value of R_A? **(06 Marks)**

OR

6 a. Analyze the working of a Schmitt trigger circuit and also design a Schmitt trigger circuit with UTP = +5V, LTP = –5V with $\pm V_{sat} = \pm 15V$. Draw its input, output and hysteresis curve. **(10 Marks)**

b. Understand and explain the working of zero crossing detector with relevant circuit and necessary waveforms. **(06 Marks)**

Module-4

7 a. Design a CMOS NOR gate and also mention the advantages of CMOS logic. **(06 Marks)**

b. Realize a EX-OR gate using NAND and NOR gates only. **(06 Marks)**

c. Realize AND gate using diode. **(04 Marks)**

OR

8 a. Create a MOD 9 upcounter. **(08 Marks)**

b. With a neat circuit diagram describe the operation of a JK Flip Flop. Write truth table, timing diagram and also mention the drawback of it. **(08 Marks)**

Module-5

9 a. Implement the following Boolean function using the depth understanding of MUX.

$f(x, y, z) = \varepsilon m(1, 2, 4, 6, 7)$ **(06 Marks)**

b. Analyze the working of successive approximation type ADC with neat sketch. Also obtain the 4 bit binary representation of analog signal 10-7 V using successive approximation technique. Full scale voltage = ±16V. **(10 Marks)**

OR

10 a. Discuss the operation of weighted resistor 4 bit DAC with necessary circuit and equations. **(06 Marks)**

b. Analyze the working of 2 × 4 decoder circuit and also design a 3 × 8 decoder using 2 × 4 decoder. **(10 Marks)**

* * * * *