FPGA and ASIC Implementation of 16-Bit Vedic Multiplier Using Urdhva Triyakbhyam Sutra

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Abstract The ever increasing demand in enhancing the ability of processors to handle the complex and challenging processes has resulted in the integration of a number of processor cores into one chip. Still the load on the processor is not less in generic system. This load is reduced by supplementing the main processor with coprocessors, which are designed to work upon specific type of functions like numeric computation, signal processing, and graphics. The speed of arithmetic logic unit (ALU) depends greatly on the multiplier. In algorithmic and structural levels, numerous multiplication techniques have been developed to enhance the efficiency of the multiplier which concentrates in reducing the partial products and the methods of their addition but the principle behind multiplication remains the same in all cases. Vedic mathematics [1] is the ancient system of mathematics which has a unique technique of calculations based on 16 sutras. Employing these techniques in the computation algorithms of the coprocessor will reduce the complexity, execution time, area, power, etc. Our work has proved the efficiency of Urdhva Triyagbhyam—Vedic method for multiplication which strikes a difference in the actual process of multiplication itself. It enables parallel generation of intermediate products. This sutra is to be used to build a high-speed power-efficient multiplier in the multiply-accumulate (MAC) unit. First, field programmable gate array (FPGA) realization is achieved and next standard cell–based ASIC design of the multiplier is realized. In 180 nm CMOS technology, our speed is 5.2 ns, 257 uW, and its using 1,117 cells.

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