CBCS SCHEME

USN | | | | | | | | | | |

17EC34

Third Semester B.E. Degree Examination, June/July 2019
Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Construct a truth table and write a Boolean expression for the problem statement. An output variable Y is to be true when the value of inputs exceeds 4. The weights for each input variable is a = 4, b = 3, c = –1, and d = 1. Design the logic circuit for the obtained expression. **(10 Marks)**

b. Place the equation $P = f(a,b,c) = ab + \bar{a}c + b\bar{c}$ into proper canonical form and write the minterms. **(05 Marks)**

c. What do you mean by canonical SOP and canonical POS? Explain with example? **(05 Marks)**

OR

2 a. Simplify K = f(w, x, y, z) = Σm(0, 1, 5, 13, 15) + Σd(2, 7, 10, 14) using K-map method. Draw the logic diagram for obtained expression. **(10 Marks)**

b. Simplify D = f(a, b, c, d) = Σm(0, 1, 2, 3, 6, 7, 8, 9, 12, 15) using QM – method, verify the same using K–map. Draw the logic diagram for simplified expression. **(10 Marks)**

Module-2

3 a. What is an encoder? Design 4 to 2 priority encoder? **(08 Marks)**

b. Realize the function X = f(a, b, c, d) = Σm(0, 3, 7, 10, 13) using 74LS138 ICs. **(08 Marks)**

c. Design 4 : 1 Mux and draw the logic diagram using basic gates. **(04 Marks)**

OR

4 a. Implement f(a, b, c, d) = Σm(0, 1, 5, 6, 7, 10, 15) using 8 : 1 Mux with a, b, c as select lines. **(08 Marks)**

b. Design a binary full subtractor using NAND gates only. **(06 Marks)**

c. Explain about carry look ahead adder. **(06 Marks)**

Module-3

5 a. Obtain the characteristic equations for D and T flip-flops. **(08 Marks)**

b. Explain the operation of SR–Flip-Flop with the help of logic diagram. Draw functional table. **(08 Marks)**

c. What is race around condition? Explain with diagram. **(04 Marks)**

OR

6 a. Explain the working of master slave J-K flip flop with the help of logic diagram. Draw the timing diagrams of the same. **(10 Marks)**

b. Explain D-flip-flop operation using positive edge triggered clock. **(06 Marks)**

c. Write two-two difference between :
i) Combinational and sequential logic
ii) Latch and flip-flop. **(04 Marks)**

Module-4

7 a. What is register? Explain with diagram of 4-bit serial-in parallel-out shift register. **(10 Marks)**

b. Explain 3-bit asynchronous up and down binary counters. **(10 Marks)**

OR

8 a. Design mod-5 ripple counter using T-flip-flops. **(08 Marks)**

b. Design 3-bit synchronous up counter. **(08 Marks)**

c. Compare asynchronous and synchronous counters. **(04 Marks)**

Module-5

9 a. Design a Mealy type sequence detector to detect a serial input sequence of 101. **(10 Marks)**

b. Design 2-bit synchronous up counter. **(10 Marks)**

OR

10 a. Analyze the following sequential circuit, by writing input and output equations, state table and state diagram. **(12 Marks)**

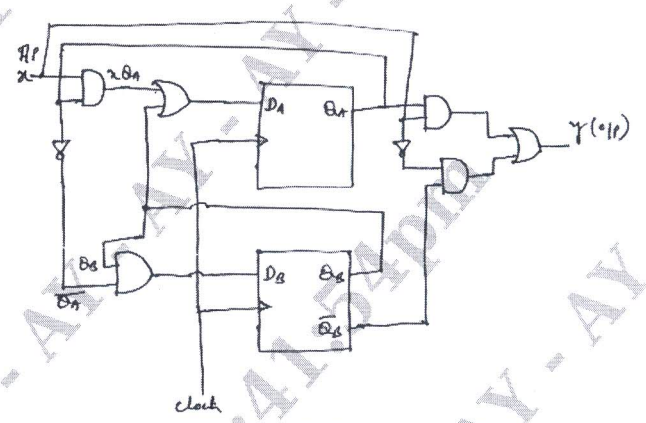

Fig.Q10(a)

b. What are Mealy and Moore models? Explain briefly with diagram. **(04 Marks)**

c. Draw a sate table and state diagram with an example. **(04 Marks)**

* * * * *