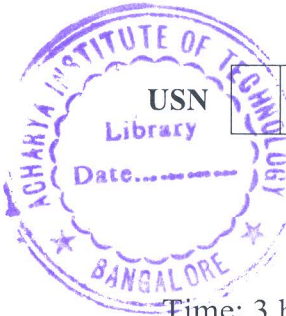


CBCS SCHEME



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15MT36

Third Semester B.E. Degree Examination, June/July 2019

Computer Organization

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Describe with necessary block diagram the basic functional unit of a computer. (08 Marks)
- b. What is a Bus? Describe with single bus structure used to interconnect functional units in computer system. (08 Marks)

OR

- 2 a. Design BIG-ENDIAN and LITTLE-ENDIAN methods of byte Addressing with proper example. (08 Marks)
- b. The register R1 and R2 contain Decimal Values 1200 and 1400. Explain following instructions:
 - i) MOVE # 3000, R5
 - ii) STORE R5, 30 (R1, R2)
 - iii) ADD (R2), R5
 - iv) ADD R1, R2, R3
 (08 Marks)

Module-2

- 3 a. Describe addressing mode. Explain the following with an example for each:
 - i) Immediate AM
 - ii) Indirect AM
 - iii) Auto Increment AM
 - iv) Relative AM. (08 Marks)
- b. Describe the operation of stack with an example. (08 Marks)

OR

- 4 a. Describe with diagram of the basic input, output operation. (10 Marks)
- b. Describe with neat block diagram of subroutine linkage using link register. (06 Marks)

Module-3

- 5 a. Describe the arrangement for Bus Arbitration using a Centralized and Distributed Arbitration. (10 Marks)
- b. What is DMA? Explain the registers in a DMA interface. (06 Marks)

OR

- 6 a. With a block describe a general 8-bit parallel interface. (08 Marks)
- b. Describe architecture and protocols with respect to USB. (08 Marks)

Module-4

- 7 a. Design the internal organization of 16M bit DRAM chip configured 2m × 8 cells. (08 Marks)
- b. Design and explain with neat diagram of synchronous DRAM. (08 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
 2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

OR

- 8 a. Describe Virtual Memory. With a diagram, explain how Virtual memory is address translated. (08 Marks)
- b. With neat diagram describe direct mapping cache memory. (08 Marks)

Module-5

- 9 a. Describe with neat diagram of 3-bus organization of the data path. (08 Marks)
- b. With neat diagram describe the hardwired control unit. (08 Marks)

OR

- 10 a. Design with neat block diagram of A compete processor. (08 Marks)
- b. Describe with example of microprogrammed control unit. (08 Marks)
