CBCS SCHEME

USN | | | | | | | | | | 17MT36

Third Semester B.E. Degree Examination, June/July 2019
Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Write the basic functional units of a computer and explain function of each of units. **(10 Marks)**

b. Draw and explain the connection between memory and processor with the respective registers. **(10 Marks)**

OR

2 a. Discuss the performance equation of the processor. **(05 Marks)**

b. List the different systems used to represent signed numbers perform the following operations on a 4 bit signed numbers using 2's complement representation system:
i) (+2) + (+3) ii) (+4) + (–6) iii) (–7) – (–5) **(05 Marks)**

c. Explain with neat time line diagram, how the user program and OS routine share the processor for reading a machine level language data and print the results. Explain how the multitasking can be made possible for the same processor. **(10 Marks)**

Module-2

3 a. Define an addressing mode. Explain four addressing mode with an example. **(10 Marks)**

b. Explain the principle of operation of stack with suitable instruction and diagram. **(10 Marks)**

OR

4 a. There are n = 100 numbers stored in the memory location starting from NUM 1 at 208. Each of the numbers is word organized. It is required to add these numbers and store at memory location SUM. Write assembly language program to perform this task. Use the necessary assembler directive. **(10 Marks)**

b. What is subroutine linkage? With example explain different ways of passing parameter to subroutine. **(10 Marks)**

Module-3

5 a. Write an assembly language program to read a line of characters from the key board, terminated by carriage return. Store the characters in memory buffer and echo it back to the display. Use status bits to accept the character from keyboard and send character to display. **(10 Marks)**

b. Explain the principle of DMA and also explain DMA concept. **(10 Marks)**

OR

6 a. What is an interrupt? List the sequence of events involved in handling an interrupt request from a single device. **(05 Marks)**

b. With the help of diagram, explain the Daisy Chain interrupt priority scheme. **(05 Marks)**

c. Discuss briefly the protocols of USB. **(10 Marks)**

Module-4

7 a. Write a CMOS memory cell and explain the write and read operation of the cell. (08 Marks)
b. Discuss the internal organization of 2M × 8 asynchronous DRAM chip. (10 Marks)
c. Write types of ROM. (02 Marks)

OR

8 a. Explain direct and set associative mapping between cache and main memory. (10 Marks)
b. What is virtual memory? With neat diagram explain how virtual memory address translated. (10 Marks)

Module-5

9 a. Write the single bus organization of the data paths inside a processor and explain the importance of each unit. (10 Marks)
b. Write the control sequence for an unconditional branch instruction and explain. (10 Marks)

OR

10 a. Write the input and output gating of registers for the operation Add R_1, R_2, R_3 during execution phase and explain the operation. (10 Marks)
b. Write the block diagram of Hardwired control unit organization and explain the importance of each unit. (10 Marks)

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