CBCS SCHEME

USN | | | | | | | | | |

15MT62

Sixth Semester B.E. Degree Examination, June/July 2019
Embedded Systems (ARM)

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. List out and explain RISC design philosophy and also describe how instruction set differs from pure RISC instruction set. **(10 Marks)**

b. Explain current program status register of ARM with neat sketch. **(06 Marks)**

OR

2 a. Discuss the core-extensions concept with necessary sketch. **(10 Marks)**

b. Explain Exceptions, interrupts and vector table in ARM. **(06 Marks)**

Module-2

3 a. Explain the following ARM instructions
   i) Arithmetic instructions
   ii) Logical instructions
   iii) Comparison instructions. **(09 Marks)**

b. Explain single register load store addressing modus for ARM instruction set with example. **(07 Marks)**

OR

4 a. Explains ARM – Thumb interworking with suitable example code. **(08 Marks)**

b. Explain the following thumb instructions
   i) Stack instructions
   ii) Multiple register load store instructions. **(08 Marks)**

Module-3

5 a. Explain the following with examples for each
   i) One cycle interlock caused by load instruction
   ii) Pipeline flush caused by branch **(06 Marks)**

b. With the help of example code show how scheduling of load instructions inserts stall. And also explain how load scheduling by preloading improves efficiency. **(10 Marks)**

OR

6 Explain the following ;
   i) Allocating variables to register numbers
   ii) Fixed width Bit field packing and unpacking
   iii) Decremented counted loops
   iv) Profiling and cycle counting. **(16 Marks)**

Module-4

7 a. Explain how main memory maps to a direct mapped cache. **(08 Marks)**

b. Explain logical and physical cache with neat sketch. **(08 Marks)**

OR

8 Explain the following with reference to cache
   i) Hit rate and miss rate
   ii) Write through and write back
   iii) Cache line replacement policies
   iv) Read allocate and read write allocate. **(16 Marks)**

Module-5

9 a. Explain about non-nested interrupt handler and nested interrupt handler scheme. **(12 Marks)**
   b. Explain about Exception priorities. **(04 Marks)**

OR

10 a. Explain about prioritized simple interrupt landler with flow chart. **(08 Marks)**
   b. Explain the following concept.
      i) ARM processor Exceptions and modes
      ii) Link register offsets. **(08 Marks)**

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