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10ES32

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
Analog Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note: *Answer FIVE full questions, selecting atleast TWO questions from each part.*

PART – A

1 a. Explain the fallowing with respect to a semi conductor diode.
i)Transition capacitance ii) Reverse necessary time iii) Piece-wise linear model. **(06 Marks)**

b. For the circuit shown in Fig.Q1(b) Find and plot the waveforms of 'V_0' for the input indicated. **(06 Marks)**

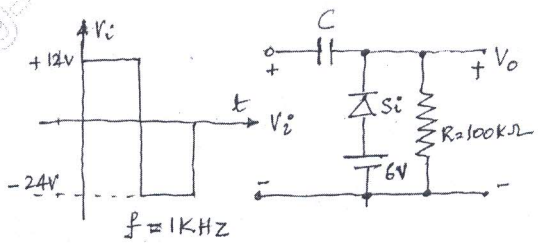

Fig.Q1(b)

c. For the circuit shown in Fig.Q1(c) :
i) Explain the operation of the circuit
ii) Calculate DC o/p voltage and current
iii) Find average and peak diode currents.
iv) Calculate the required PIV rating of each diode.
Assume ideal diodes and take $R_1 = R_2 = R = 10k\Omega$. **(08 Marks)**

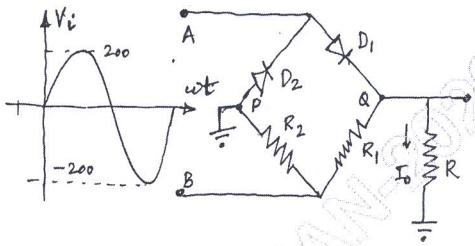

Fig.Q1(c)

2 a. Derive an expression for stability factor $S(I_{CO})$ and $S(V_{BE})$ for collector feedback bias. **(09 Marks)**

b. Design a voltage divider bias circuit using silicon transistor with $V_{CC} = 18V$, $I_C = 2.3mA$, $V_{CE} = 8.2V$, $R_C = 3.3k\Omega$, $\beta = 100$ and $S(I_{CO}) \leq 5$. **(06 Marks)**

c. For the transistor switch in shown Fig.Q2(c), $V_{BE} = 0.7V$, $(V_{CE})_{sat} = 0.3V$, $I_{CE_o} = 5\mu A$ and $h_{fe} = 125$. i) Calculate $(I_C)_{sat}$ $(I_B)_{max}$, On and Off resistance $(R)_{sat}$ and $(R)_{cut\ off}$
ii) Sketch output voltage wave form. **(05 Marks)**

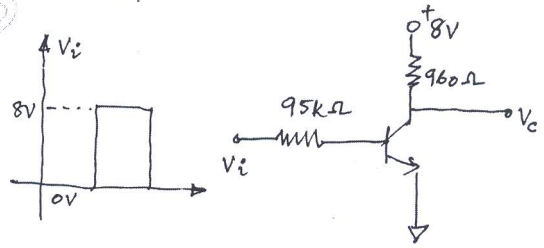

Fig.Q2(c)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

3 a. Derive an expression for Z_i, Z_0, A_V and A_I for common–base configuration using r_e model. Also discuss some applications of CB configuration. **(10 Marks)**

b. For the emitter follower circuit shown in Fig.Q3(b), calculate r_e, Z_i, Z_0 A_V and A_I. Take $\beta = 100$ and $r_0 = \infty$. **(05 Marks)**

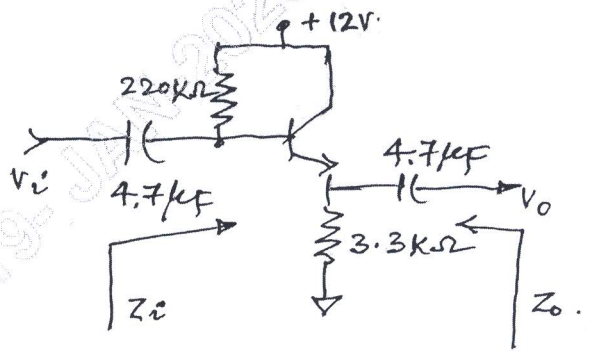

Fig.Q3(b)

c. For the circuit shown in Fig.Q3(c) below calculate r_e, Z_i, Z_0 A_V and A_I. Take $\beta = 140$ and $r_0 = 30k\Omega$.

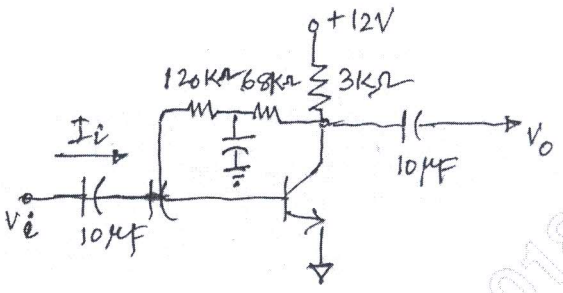

Fig.Q3(c) **(05 Marks)**

4 a. Prove that miller effect of input capacitance $C_{Mi} = (1 - A_V)C_f$ and output capacitance $C_{M0} = \left[1 - \frac{1}{A_V}\right] C_f$ and also discuss applications of Millers theorem. **(10 Marks)**

b. For the circuit shown in Fig.Q4(b) the following, using transistor with $\beta = 100$ and $r_0 = \infty\Omega$.

i) r_e

ii) input resistance R_i

iii) mid band voltage gain $A_V = V_0/V_I$ and $A_{VS} = V_0/V_S$

iv) lower cut off frequency due to C_S

v) lower cut off frequency due to C_C and C_E

vi) overall lower cut off frequency. **(10 Marks)**

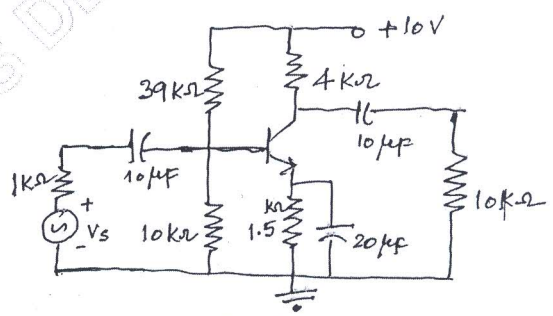

Fig.Q4(b)

PART – B

5 a. Derive expressions for Z_i and A_i for Darlington emitter follower circuit. **(08 Marks)**

b. For the current series feedback amplifier shown in Fig.Q5(b) calculate the following :

i) Densentisivity factor
ii) Transfer gain with feedback
iii) Voltage gain with and without feedback
iv) Input resistance with and without feedback
v) Output resistance with and without feedback
vi) Output current with and without feedback
vii) Output voltage with and without feedback. **(12 Marks)**

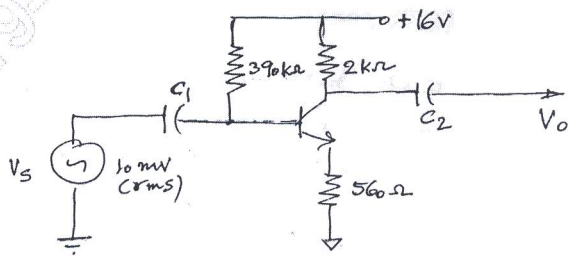

Fig.Q5(b)

6 a. Explain the operation of a class–B push pull amplifier and derive an expression for conversion efficiency. **(08 Marks)**

b. Draw the circuit of transformer coupled class A power amplifier, on performing DC and AC analysis. Derive an expression for AC power delivered to load and maximum AC output power. **(12 Marks)**

7 a. Explain the working of Wein bridge oscillator. **(06 Marks)**

b. With a neat circuit diagram, explain the operation of Hartley oscillator. **(06 Marks)**

c. Discuss the merits, demerits and application of crystal oscillators. **(04 Marks)**

d. A crystal has following parameters : L = 0.334H C = 0.065 pf C_M = 1pf R = 5.5kΩ.

i) Calculate series and parallel frequency.
ii) By what percentage does parallel resonant frequency exceeds the series resonant frequency
iii) Find the 'Q' of the crystal. **(04 Marks)**

8 a. Compare JFET and MOSFET. **(04 Marks)**

b. Draw the circuit of JFET common gate configuration. Derive an expression for Z_i, Z_0 and A_V using small signal model. Also summarize the characteristic of common gate configuration. **(10 Marks)**

c. For the JFET–common drain configuration shown in Fig.Q8(c) and for given data. Calculate Z_i, Z_0 and A_V. Find V_0 if V_i = 20 $mV_{(p-p)}$.

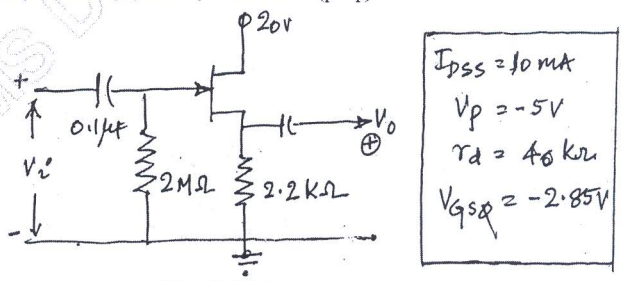

Fig.Q8(c) **(06 Marks)**

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