

# CBCS SCHEME

15EC33

## Third Semester B.E. Degree Examination, Dec.2019/Jan.2020 Digital Electronics

Time: 3 hrs.

Max. Marks: 80

*Note: Answer any FIVE full questions, choosing ONE full question from each module.*

### Module-1

- 1 a. Two motors  $M_2$  and  $M_1$  are controlled by three sensors  $S_1$ ,  $S_2$  and  $S_3$ . One motor  $M_2$  is to run any time when all three sensors are on the other motor ( $M_1$ ) is to run whenever sensors  $S_2$  or  $S_1$  but not both are on and  $S_3$  is off. For all sensors combinations where  $M_1$  is on,  $M_2$  is to be off, except when all sensors are off and then both motors remains off. Design using combinational logic. (06 Marks)
- b. Convert the given Boolean function into minterm canonical form.  
 $f(a, b, c) = \bar{a}(\bar{b} + c) + c$  (02 Marks)
- c. Reduce the following Boolean function using K-map and realize the simplified expression using NAND gates.  
 $T = f(a, b, c, d) = \sum m(1, 3, 4, 5, 13, 15) + \sum d(8, 9, 10, 11)$  (08 Marks)

### OR

- 2 a. Determine the prime implicants and essential prime implicants for the given Boolean function using K-map.  
 $N = f(a, b, c, d) = \pi(0, 1, 4, 5, 8, 9, 11) + d(2, 10)$  (05 Marks)
- b. Define Minterm, Maxterm, Canonical POS. (03 Marks)
- c. Simplify the given function using Quine McCluskey method.  
 $f(a, b, c, d) = \sum m(7, 9, 12, 13, 14, 15) + d(4, 11)$  (08 Marks)

### Module-2

- 3 a. Design a priority encoder for a system with 3 inputs, the middle bit with highest priority encoding to 10, the MSB with next priority encoding to 11, while the LSB with last priority encoding to 01. (05 Marks)
- b. Realize the following Boolean function using 8 to 1 MUX.  
 $f(a, b, c, d) = \sum m(0, 1, 5, 6, 7, 10, 15)$  (03 Marks)
- c. Design a four-bit carry look ahead adder and briefly explain how it is better than parallel adder. (08 Marks)

### OR

- 4 a. Realize a 16:1 MUX using 4:1 Multiplexers only. (03 Marks)
- b. Implement the given function using 74139 dual 2:4 decoder  
 $f_1(a, b, c) = \pi(1, 3, 5, 7)$  (03 Marks)
- c. Design two-bit binary comparator and implement with suitable logic gates. (10 Marks)

### Module-3

- 5 a. What is the difference between combinational logic and sequential logic? Explain switch debouncer using SR latch with waveforms. (08 Marks)
- b. Explain the working of Master-Slave JK flip-flop with the help of logic diagram, function table, logic symbol and timing diagram. (08 Marks)

OR

- 6 a. What is race around condition and how this can be eliminated? (03 Marks)
- b. Obtain the characteristic equation of JK and SR flip-flops. (05 Marks)
- c. Explain the working of positive edge triggered D flip-flop with neat logic diagram and waveforms. (08 Marks)

**Module-4**

- 7 a. Explain Universal Shift Register with the help of logic diagram, mode control table and symbol. (08 Marks)
- b. Explain the working of 4-bit Johnson counter using positive edge triggered D flip-flop, also draw the timing diagram. What is the modulus of this counter? (08 Marks)

OR

- 8 a. Design a synchronous Mod-6 counter using JK flip-flop. (08 Marks)
- b. Explain the working of 4-bit binary ripple up counter using negative edge triggered flip-flop also draw the timing diagram. (08 Marks)

**Module-5**

- 9 a. Explain Mealy and Moore models of clocked synchronous sequential circuits. (06 Marks)
- b. A sequential circuit has one input and one output, the state diagram is as shown in Fig.Q9(b), design the sequential circuit with JK flip-flop.

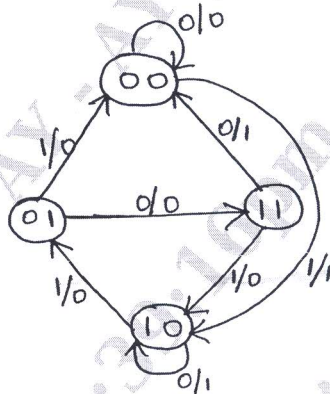


Fig.Q9(b)

(10 Marks)

OR

- 10 a. Write the basic recommended steps for design of a clocked synchronous sequential circuit. (06 Marks)
- b. Construct the excitation table, transition table, state table and state diagram for the Moore sequential circuit shown in Fig.Q10(b).

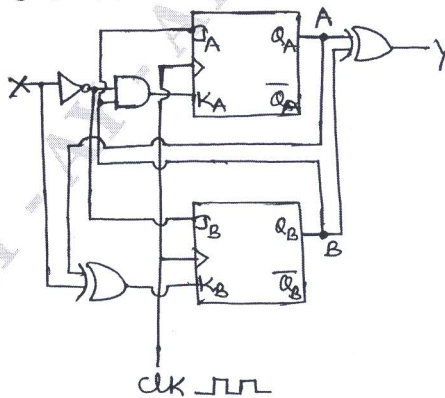


Fig.Q10(b)

(10 Marks)

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