



Fifth Semester B.E. Degree Examination, Dec.2019/Jan.2020

Fundamentals of CMOS VLSI

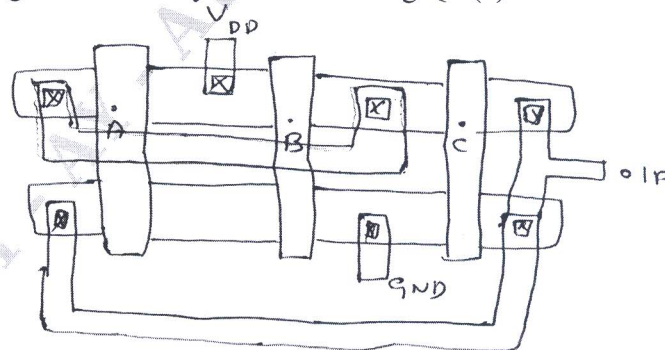
Max. Marks:100

Note: Answer any FIVE full questions, selecting at least TWO full questions from each part.

PART - A

- 1 a. Explain the enhancement transistor action of MOSFET DEVICE. Draw its output characteristics, mention the region of operation. (10 Marks)
 b. Explain fabrication of CMOS using nwell process. (06 Marks)
 c. Compare the CMOS with BiCMOS technology. (04 Marks)
- 2 a. Draw the DC characteristics of CMOS inverter, mention the region of operation. Derive the mid-point voltage equation for CMOS inverter. Discuss the effect of B_n/B_p ratio on DC characteristics. (12 Marks)
 b. A NMOS transistor is operating with following parameter:
 $V_{GS} = 3.9V$ $U_{th} = 1V$, $W/L = 100$
 $\mu_n C_{ox} = 90 \mu A/V^2$ find I_D for i) $V_{DS} = 5U$ ii) $U_{DS} = 2.1V$. (08 Marks)
- 3 a. Describe the pass characteristics of nMOS and pMOS device. Realize 2 input XOR gate with pass transistor and CMOS. (06 Marks)
 b. Draw the schematic diagram and stick diagram for Boolean expression $y = \overline{(A+B)C}$ using CMOS logic. Use colour/monochromatic codes. (06 Marks)
 c. Realize $\overline{(A+B)(C+D)}$ using
 i) Pseudo nMOS logic
 ii) Dynamic CMOS logic
 iii) CMOS logic
 iv) Domino logic. (08 Marks)
- 4 a. What is mean by λ -based design rule represent each layers of CMOS with it standard colour code and dimension as per the design rule. (06 Marks)
 b. Discuss the advantages and disadvantages of scaling the MOS device. Derive the scaling factor for following:
 i) Gate delay
 ii) Carrier density in the channel
 iii) Channel resistance R_{on} . (08 Marks)
 c. Draw the circuit diagram for the layout shown in Fig.Q.4(c). (06 Marks)

Fig.Q.4(c)



PART – B

- 5 a. Differentiate between pass transistor and transmission gate. (04 Marks)
 b. In the circuit shown in the Fig.Q.5(b). Find V_1 , V_2 , V_3 and V_4 . Justify your answer
 $V_{DD} = 5V$, $V_{24} = 0.7V$. (06 Marks)

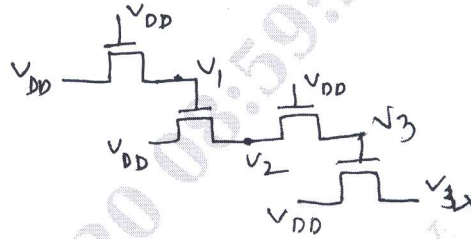


Fig.Q.5(b)

- c. Draw the schematic diagram of BiCMOS 3 input NOR gate. Explain circuit operation. Draw the stick diagram for the same. (10 Marks)
- 6 a. What is mean by C^2 MOS logic (clocked CMOS). Illustrate with example of 2 i/p x – OR gate. (08 Marks)
 b. Explain the design of 4 bit barrel shifter with neat diagram. (12 Marks)
- 7 a. Explain how ALU functions can be implemented with adder. (10 Marks)
 b. Explain with block diagram carry look ahead adder. (10 Marks)
- 8 a. Explain nMOS and CMOS pseudo-static memory cell with relevant diagram. (10 Marks)
 b. Mention the performance parameters of design process. Explain optimization of nMOS and CMOS inverter. (10 Marks)
