CBCS SCHEME

USN 1 A Y 1 6 M T 0 3 5

15MT36

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
Computer Organization

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. What is bus? Explain the advantage and disadvantage of single bus structure with a neat diagram. **(06 Marks)**

b. Write the basic performance equation. Explain the role of each of the parameter in the equation. **(04 Marks)**

c. What are the basic instruction types? Explain with example. **(06 Marks)**

OR

2 a. Explain the connection between processor and memory, with a neat diagram. **(08 Marks)**

b. What is byte addressability? Explain Big-endian and Little-endian assignment with example. **(08 Marks)**

Module-2

3 a. What is addressing mode? Explain any four addressing modes with example. **(08 Marks)**

b. What is subroutine linkage method? Explain subroutine linkage using link register. **(08 Marks)**

OR

4 a. What are assembler directives? Explain with example program. **(08 Marks)**

b. Discuss various logical shift and rotate instructions with example. **(08 Marks)**

Module-3

5 a. What is interrupt service routine? Explain the concept of interrupt nesting with a neat diagram. **(08 Marks)**

b. With a neat timing diagram explain how input transfer happens on a synchronous bus. **(08 Marks)**

OR

6 a. What is DMA approach? Explain in detail. **(08 Marks)**

b. With a neat diagram, explain how simultaneous interrupt requests are handled. **(08 Marks)**

Module-4

7 a. With a neat diagram, explain the working of 1KX1 memory chip. **(06 Marks)**

b. Explain the concept of memory interleaving with neat diagram. **(06 Marks)**

c. What is virtual memory technique? Draw the neat diagram of virtual memory organization. **(04 Marks)**

OR

8 a. What is ROM? Explain various types of ROM. **(08 Marks)**

b. Explain synchronous DRAM operation with a neat block diagram. **(08 Marks)**

Module-5

9 a. Discuss single bus organization of a processor, with a neat diagram. **(08 Marks)**

b. Give a detailed diagram of hardwired control unit and explain its organization. **(08 Marks)**

OR

10 a. Explain three bus organization of a processor with a neat diagram. **(08 Marks)**

b. Discuss the basic organization of a microprogrammed control unit with a neat diagram. **(08 Marks)**

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