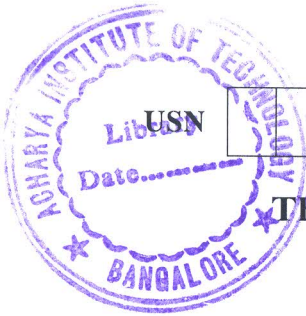


CBCS SCHEME

17MT36



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Third Semester B.E. Degree Examination, Dec.2019/Jan.2020 Computer Organization

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Explain the different functional units of computer with a neat block diagram. (08 Marks)
- b. What is bus? Explain the advantages and disadvantages of single bus structure with a neat diagram. (06 Marks)
- c. Write a basic performance equation and explain the parameters that affect the overall performance of the system. (06 Marks)

OR

- 2 a. Explain the connection between processor and memory with a neat diagram. (06 Marks)
- b. What is straight line sequencing? Explain with example program. (06 Marks)
- c. What is byte addressability? Explain Big-endian and Little-endian assignment with example. (08 Marks)

Module-2

- 3 a. Define addressing mode. Explain any three addressing mode with example. (10 Marks)
- b. What is Stack? Write a routine for safe push and pop operation. (05 Marks)
- c. Explain with example program how parameters are passed to subroutine using registers. (05 Marks)

OR

- 4 a. What is subroutine linkage method? Explain with example. (06 Marks)
- b. Explain program controlled I/O operation with a neat diagram. (06 Marks)
- c. What are assembler directives? Explain its use with assembly language program. (08 Marks)

Module-3

- 5 a. Discuss the different schemes available to enable and disable interrupts. (06 Marks)
- b. Explain how simultaneous interrupt requests from several I/O devices will be handled by a processor using daisy chain arrangement. (06 Marks)
- c. With a neat timing diagram, explain how data transfer happens during input operation over asynchronous bus. (08 Marks)

OR

- 6 a. What is interrupt service routine? Explain the concept of interrupt nesting with a neat diagram. (08 Marks)
- b. What is DMA approach? Explain. (06 Marks)
- c. Explain with a neat diagram, how interrupt hardware circuit is used to implement a common interrupt request line. (06 Marks)

Module-4

- 7 a. Explain the working of single transistor dynamic memory cell with a neat diagram. (06 Marks)

- b. Explain the concept of memory interleaving with a neat diagram. (06 Marks)
c. What is ROM? Explain various types of ROM. (08 Marks)

OR

- 8 a. Explain the internal organization of $2m \times 8$ dynamic memory chip with a neat diagram. (06 Marks)
b. What is virtual memory technique? Explain the organization of virtual memory with a neat diagram. (06 Marks)
c. Explain direct mapped cache and associative mapped cache with neat block diagram. (08 Marks)

Module-5

- 9 a. Draw and explain the single bus organization of the datapath inside a processor. (08 Marks)
b. Explain control sequence for an un-conditional branch instruction. (06 Marks)
c. Explain with block diagram the basic organization of microprogrammed control unit. (06 Marks)

OR

- 10 a. Draw and explain multiple bus organization of CPU. (08 Marks)
b. Write a control sequence for execution of the instruction Add (R_3), R_1 . (06 Marks)
c. Explain hardwired control unit organization with a neat diagram. (06 Marks)

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