CBCS SCHEME

USN | | | | | | | | | | |

17EE35

Third Semester B.E. Degree Examination, Aug./Sept.2020
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Convert the following equations into proper canonical form:
i) f(A, B, C) = A + ABC into standard SOP form.
ii) f(A, B, C) = A.(A + B + C) into standard POS form. **(10 Marks)**

b. Reduce the following function using K-Map technique:
f(A, B, C, D, E) = $\sum$m (1, 4, 8, 10, 11, 20, 22, 24, 25, 26) + $\sum$d(0, 12, 16, 17) **(10 Marks)**

OR

2 a. Simply the following using Quine-McCluskey method:
f(A, B, C, D) = $\sum$m(1, 2, 3, 5, 9, 12, 14, 15) + $\sum$d(4, 8, 11) **(10 Marks)**

b. Design a logic circuit with inputs P, Q, R so that output Y is high whenever P is zero or whenever Q = R = 1. **(10 Marks)**

Module-2

3 a. i) Implement f(A, B, C) = $\sum$m(1, 3, 5, 6) using 4:1 multiplexer.
ii) Implement f(P, Q, R, S) = $\sum$m(0, 1, 3, 4, 8, 9, 15) using 8:1 multiplexer. **(10 Marks)**

b. Explain the concept of look ahead adder and hence realize 3 bit parallel adder using Look ahead carry generator. **(10 Marks)**

OR

4 a. Implement full subtractor using 3:8 decoder. **(10 Marks)**

b. Design 2-bit magnitude comparator using gates. **(10 Marks)**

Module-3

5 a. Explain the operation of gated S-R flipflop using NAND gates, with truth table. **(10 Marks)**

b. Design synchronous MOD-6 counter using S-R flip flop. **(10 Marks)**

OR

6 a. With logic diagram, explain the working of master slave J-K flip flop along with waveforms. Explain about race around condition. **(10 Marks)**

b. Design synchronous mod-3 counter using J-K flip flop. **(10 Marks)**

Module-4

7 a. Construct the transition table, state table and state diagram for the given synchronous sequential circuit. **(10 Marks)**

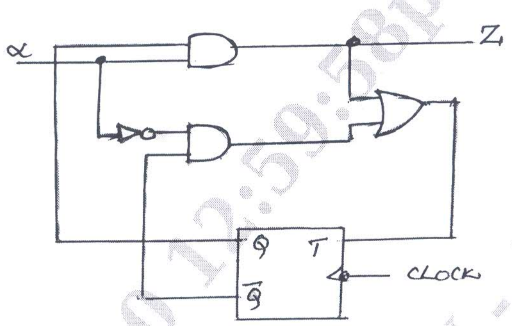

Fig.Q.7(a)

b. Obtain transition table and excitation table for the given state diagram. **(10 Marks)**

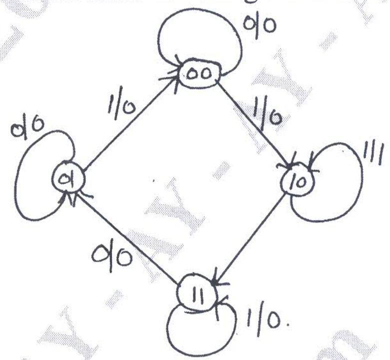

Fig.Q7(b)

OR

8 a. Construct the transition table, state table and state diagram for the Moore sequential circuit. **(12 Marks)**

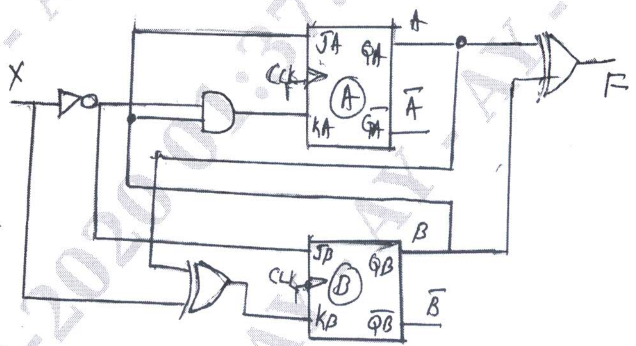

Fig.Q.8(a)

b. Compare Moore model and Mealy Model. **(08 Marks)**

Module-5

9 a. Write data flow description for full adder in both VHDL and verilog. **(10 Marks)**

b. Compare VHDL and verilog. **(10 Marks)**

OR

10 a. Describe different operators in VHDL and verilog. **(10 Marks)**

b. Briefly describe different styles of descriptions in VHDL. **(10 Marks)**

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