



CBCS SCHEME

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15EC63

Sixth Semester B.E. Degree Examination, Aug./Sept. 2020

VLSI Design

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Explain the ideal I.V characteristics of nMOS transistor. Derive the equation for I_{DS} in three region i) cut off region ii) non-saturated region iii) saturation region. (10 Marks)
b. Explain the nMOS fabrication with neat diagram. (06 Marks)

OR

- 2 a. Explain the CMOS inverter transfer characteristics highlighting the regions of operations of the MOS transistor. (06 Marks)
b. Describe with neat sketches the fabrication of P-well CMOS inverter. (06 Marks)
c. Compare CMOS and bipolar technology. (04 Marks)

Module-2

- 3 a. Draw the circuit schematic and stick diagram of CMOS 2 input NAND gate. (08 Marks)
b. Explain briefly λ -based design rules for wire and transistor (nMOS, PMOS, CMOS). (08 Marks)

OR

- 4 a. Explain with diagram rise time model and fall time model of CMOS inverter. (06 Marks)
b. Explain briefly the circuit of inverting and non-inverting super buffer. (06 Marks)
c. Explain delay unit τ . (04 Marks)

Module-3

- 5 a. What are the most commonly used scaling models? Provide scaling factor for :
i) Power dissipation per gate ii) Current density
iii) Channel resistance R_{on} iv) Parasitic capacitance C_x . (06 Marks)
b. What are the general considerations to be followed in designing a sub system? (05 Marks)
c. Explain the design steps for 4-bit adder. (05 Marks)

OR

- 6 a. Design regularity. (04 Marks)
b. Design 4 bit ALU to implement addition subtraction, EX-OR, EX-NOR and AND operation. (12 Marks)

Module-4

- 7 a. Discuss the architectural issue related to sub system design. (06 Marks)
b. Explain briefly a parity generator with block diagram and stick diagram. (06 Marks)
c. Give the comparison of SSRAM and antifuse FPGA. (04 Marks)

OR

- 8 a. Explain with schematic view of flash based FPGA. (05 Marks)
b. Explain briefly switch logic implementing of a four way multiplexer. (07 Marks)
c. What are the advantages of FPGA? (04 Marks)

Module-5

- 9 a. Explain the three transistor dynamic RAM – cell. (08 Marks)
b. Explain briefly nMOS Pseudo static memory cell. (08 Marks)

OR

- 10 a. Explain briefly logic verification principle. (08 Marks)
b. Write a short note on : i) Built In Self Test (BIST) ii) Scan Design Technology. (08 Marks)

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Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.