CBCS SCHEME

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18EE35

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define combinational logic. List the various steps in designing the combinational logic circuit and explain with a block diagram. **(06 Marks)**

b. Explain the canonical minterm and maxterm form with examples. **(04 Marks)**

c. Simplify the Boolean function using K-map following as
$P = f(a, b, c, d) = \Sigma m(2, 3, 4, 5, 13, 15) + \Sigma d(8, 9, 10, 11)$
$Q = f(w, x, y, z) = \pi(1, 4, 5, 11, 12, 13, 14, 15) \cdot d(3, 9, 10)$. **(10 Marks)**

OR

2 a. Using K-map method, obtain a minimal SOP expression and implement the function using NAND gates.
$x = f(a, b, c, d, e) = \Sigma m(1, 3, 4, 6, 9, 11, 12, 14, 17, 19, 20, 22, 25, 27, 28, 30)$. **(08 Marks)**

b. Simplify using Quire – McCluskey method and realize the function using a basic gates.
$M = f(a, b, c, d) = \Sigma m(7, 9, 12, 13, 14, 15) + \Sigma d(4, 11)$. **(12 Marks)**

Module-2

3 a. Design a combinational logic circuit that will convert BCD digit to Excess-3 BCD digit using gates. Construct a truth table and simplify each output equation using K-maps. **(08 Marks)**

b. Design a binary full adder using only 2-input NAND gates. Construct a truth table and write a Boolean expression for SUM and CARRY. **(07 Marks)**

c. Design a 4 to 16 line decoder by cascading 2 to 4 line decoders which has the active low output and active low enable input. **(05 Marks)**

OR

4 a. Realize the following Boolean function using 8 : 1 MUX with 'wyz' as select inputs.
$V = f(w, x, y, z) = \Sigma m(0, 1, 2, 5, 7, 8, 9, 12, 13)$. **(05 Marks)**

b. Implement 4 bit parallel adder/subtract using 4-full adders blocks. Explain its operation if $C_{in} = 0$ the circuit should act as adder and if $C_{in} = 1$ the circuit act as subtractor. **(05 Marks)**

c. Design a two-bit magnitude comparator with help of the truth table and simplification of the output equations using K-maps. Draw a logic diagram. **(10 Marks)**

Module-3

5 a. Explain the operation of SR Latch act as switch debouncer with help of the timing diagram. **(05 Marks)**

b. Explain the working of a Master-slave JK flip-flop with a neat logic diagram, function table, logic symbol and timing diagram. **(10 Marks)**

c. Obtain the characteristic equation of the JK and D flip-flops. **(05 Marks)**

OR

6 a. Differentiate the sequential logic circuit and combinational logic circuit. **(04 Marks)**

b. Explain the operation of SR latch with a neat logic diagram and timing diagram. **(06 Marks)**

c. Draw a neat diagram and explain the working of positive edge-trigger D-flipflop with function table, logic symbol and timing diagram. **(10 Marks)**

Module-4

7 a. Explain the working of 4-bit binary ripple counter using a positive edge trigger T-flip-flop with an enable line and relevant timing diagram. **(08 Marks)**

b. Design a mod-8 twisted ring counter and explain its operation. Write the count sequence table. **(07 Marks)**

c. With a neat logic diagram, explain the operation of the 4-bit SISO unidirectional shift register. **(05 Marks)**

OR

8 a. Design a synchronous counter with counting sequence. 3, 2, 5, 1, 0, 3 . . . . using D-flip-flips. **(10 Marks)**

b. With a neat logic diagram, explain the 4-bit universal shift register using D-flip-flops and a 4 : 1 MUX. Write a mode control and register operation. **(10 Marks)**

Module-5

9 a. With a suitable block diagram, explain the Mealy and Moore model in a sequential circuit analysis. **(08 Marks)**

b. Construct a sequential logic circuit with single input(x) and single output(z) by obtaining the state and excitation tables for the given state diagram as shown in Fig.Q9(b), using JK flip-flops.

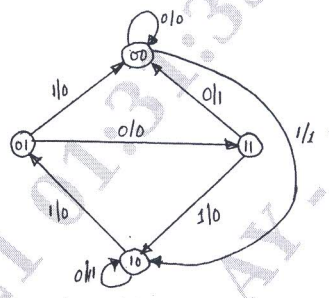

Fig.9(b) **(12 Marks)**

OR

10 a. Differentiate a Mealy and Moore models. **(04 Marks)**

b. Explain the following terms : i) ROM ii) PROM iii) Flash memory with a suitable diagram. **(06 Marks)**

c. Analyze the following sequential logic circuit as shown in Fig.Q10(c). Obtain the excitation and output equation, transition table and state table. Also draw a state diagram.

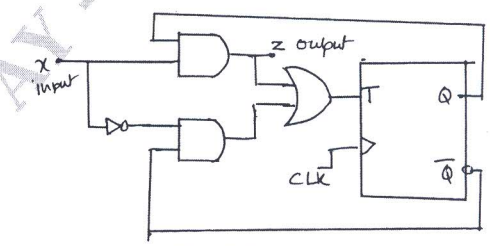

Fig.Q10(c) **(10 Marks)**

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