CBCS SCHEME

USN | | | | | | | | | | |

17EC33

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Analog Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. What is BJT transistor modeling? Obtain the expression for voltage gain, Z_{in} and Z_o of CB configuration using AC equivalent circuit with re model. **(05 Marks)**

b. Derive the expression for A_i, A_v, Z_i and Z_o for a voltage divider bias circuit of BJT, with unbypassed RE, using re equivalent model of BJT. Show the phase relationship between input and output wave form. **(10 Marks)**

c. State the characteristic features of Darlington connection. Calculate the DC bias voltages and currents in the circuit.

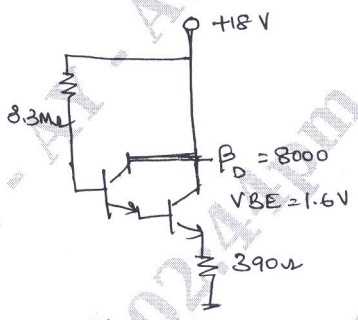

Fig.Q1(c) **(05 Marks)**

OR

2 a. Give the relation between re parameters and h parameters. What are the advantages of h parameters? **(05 Marks)**

b. Derive the expressions for current gain, voltage gain, input impedance and output impedance for an emitter follower circuit using approximate hybrid equivalent circuit. (Without the effect of r_o). **(10 Marks)**

c. For the network shown in Fig.Q2(c), determine re, Z_i, Z_o, A_v (with $r_o = \infty\Omega$) and A_v (with $r_o = 50\ K\Omega$)

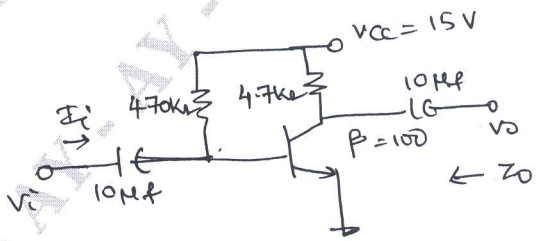

Fig.Q2(c) **(05 Marks)**

Module-2

3 a. Explain the construction of N channel JFET. Also explain the drain and transfer characteristics of the JFET. **(06 Marks)**

b. With equivalent circuit obtain the expression for Z_o and A_v for JFET self bias configuration. **(08 Marks)**

c. The fixed bias configuration shown in Fig.Q3(c) has $V_{GSQ} = -2V$, $I_{DQ} = 5.625$ mA with $I_{DSS} = 10$ mA, $V_P = -8V$ and $Y_{OS} = 40$ μS. Determine g_m, r_d, Z_o and A_v.

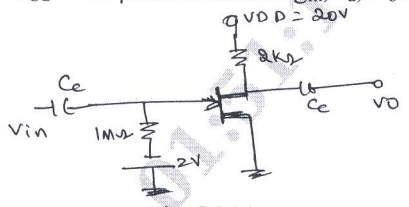

Fig.Q3(c) **(06 Marks)**

OR

4 a. Differentiate between enhancement and depletion MOSFET. **(05 Marks)**

b. With necessary equivalent circuit, obtain the expression for A_v for a JFET source follower configuration. **(05 Marks)**

c. Calculate the DC bias, voltage gain, input impedance and output impedance and resulting output voltage for the cascade amplifier shown in Fig.Q4(c). Calculate the load voltage if a 10 KΩ load is connected across the output.

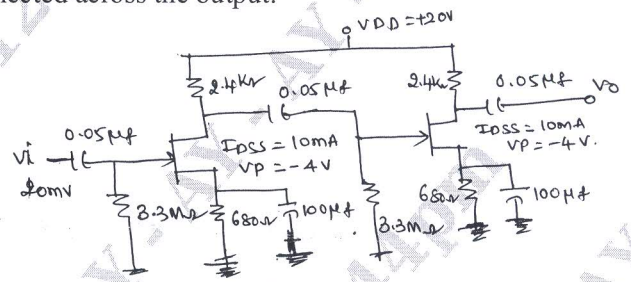

Fig.Q4(c) **(10 Marks)**

Module-3

5 a. Determine the lower cutoff frequency f_{LS} for the voltage divider bias network using the following parameters:
$C_S = 10$ μf, $C_E = 20$ μf, $C_C = 1$ μf, $R_S = 1$ KΩ, $R_1 = 40$ KΩ, $R_2 = 10$ KΩ, $R_E = 2$ KΩ, $R_C = 4$ KΩ, $R_L = 2.2$ KΩ, $\beta = 100$, $r_o = \infty\Omega$, $V_{CC} = 20$ V, re = 15.76 Ω. **(04 Marks)**

b. Explain the following: (i) Logarithm (ii) Decibel. With respect to transistor amplifier calculate the overall lower 3 dB and upper 3 dB frequencies for a 3 stage amplifier having an individual $f_1 = 40$ Hz and $f_2 = 2$ MHz. **(06 Marks)**

c. Discuss the low frequency response of BJT amplifier and give expression for lower cut off frequency due to C_C, C_E and C_S. **(10 Marks)**

OR

6 a. Draw the Hybrid π model for the transistor in CE configuration and explain the significance of each component. **(06 Marks)**

b. Describe the Miller effect and derive an equation for Miller input capacitance. **(06 Marks)**

c. Determine the high cutoff frequencies for the network shown in Fig.Q6(c).

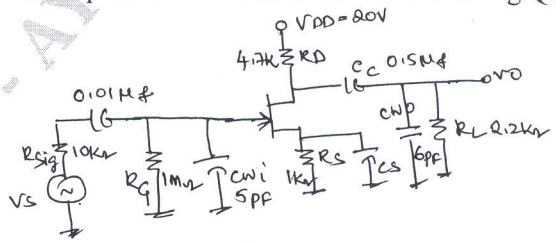

Fig.Q6(c) **(08 Marks)**

Module-4

7 a. With a block diagram, explain the concept of feedback amplifier and derive the expression for $A_f = \frac{A}{1+A\beta}$. **(06 Marks)**

b. Derive the expression for Z_{if} and Z_{of} for current series feedback amplifier. **(08 Marks)**

c. Explain a practical voltage series feedback circuit. **(06 Marks)**

OR

8 a. What is an oscillator? Discuss the concept of generating oscillations with the help of Barkhausen criteria. **(05 Marks)**

b. With a neat circuit diagram and necessary expressions, explain the Wein bridge oscillator. **(10 Marks)**

c. Design a unijunction transistor for a operation at 1 kHz and 150 kHz assuming $\eta = 0.58$. **(05 Marks)**

Module-5

9 a. Give the definition of power amplifiers and list the types of power amplifiers based on the location of Q point. **(05 Marks)**

b. Explain the working of class B complementary symmetry class B push pull amplifier. Obtain an expression for maximum conversion efficiency of this amplifier. **(10 Marks)**

c. Calculate the harmonic distortion components for an output signal having fundamental amplitude of 2.5 V, second harmonic amplitude of 0.25 V, third harmonic amplitude of 0.1 V and fourth harmonic amplitude of 0.05 V and also calculate the total harmonic distortion for the amplitude components given above. **(05 Marks)**

OR

10 a. With necessary circuit diagram and characteristic curve, explain the class-A transformer coupled amplifier. Show that the maximum efficiency can be expressed as 50%. **(10 Marks)**

b. Describe the block diagram of series and shunt type voltage regulators. **(05 Marks)**

c. Calculate the output voltage and Zener current un the regulator circuit of Fig.Q10(c) for $R_L = 5\ K\Omega$.

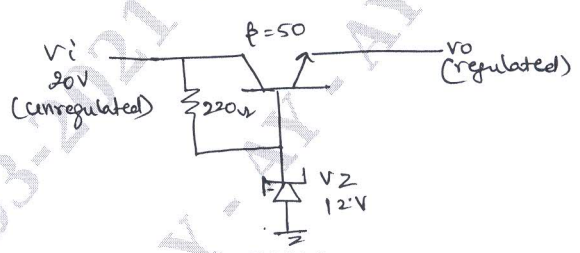

Fig.Q10(c) **(05 Marks)**

* * * * *