

Module-3

- 5 a. Design an FIR filter for the following desired frequency response

$$H_d(w) = \begin{cases} e^{-j3w}, & \text{if } |w| \leq \frac{\pi}{4} \\ 0, & \text{if } |w| > \frac{\pi}{4} \end{cases}$$

Use the Hamming window function, obtain the frequency response of the designed FIR filter. (10 Marks)

- b. For the System function $H(z) = 1 + 2.8z^{-1} + 3.4z^{-2} + 1.7z^{-3} + 0.4z^{-4}$. Obtain the Lattice coefficients and sketch the Lattice structure. (10 Marks)

OR

- 6 a. Find the Impulse response of an FIR filter with the following desired frequency response,

$$H_d(w) = \begin{cases} 0 & ; \text{ if } |w| \leq \frac{\pi}{6} \\ e^{-j4w} & ; \text{ if } |w| > \frac{\pi}{6} \end{cases}$$

Use Rectangular window function. Draw the direct form structure for the designed filter. (10 Marks)

- b. Consider an FIR Lattice filter coefficients $K_1 = 0.65$, $K_2 = 0.5$, $K_3 = 0.9$. Find its impulse response and draw the direct form structure. (10 Marks)

Module-4

- 7 a. Define the First order analog low pass filter prototype. How this prototype is transformed into a different filter types. (05 Marks)
- b. Design a Second order digital low pass Butterworth filter with a cutoff frequency of 3.4 kHz at a sampling frequency of 8000Hz. Draw the direct Form – II structure of this filter. Use Bilinear transformation. (10 Marks)
- c. Discuss the general mapping properties of bilinear transformation and show the mapping between the S – plane and the the Z – plane. (05 Marks)

OR

- 8 a. Define the Normalized low pass prototype function of Butterworth filter and derive the expression for the filter order. (05 Marks)
- b. Using Bilinear transformation, design a digital low pass Butterworth filter with the following specifications : Sampling frequency : 8000Hz , 3 dB attenuation at 1.5 kHz. 10 dB stop band attenuation at 3kHz. (10 Marks)
- c. Realize the following digital filter using direct Form – II

$$H(z) = \frac{0.7 + 1.4z^{-1} + 0.7z^{-2} + 0.5z^{-3}}{1 + 1.3z^{-1} + 0.5z^{-2} + 0.7z^{-3} + 0.3z^{-4}} \quad (05 \text{ Marks})$$

Module-5

- 9 a. With a neat diagram, explain the Harvard architecture used in DS processors. (06 Marks)
- b. Illustrate the operation of circular buffers used for address generation in DS processors. (07 Marks)
- c. Convert the following decimal numbers into the floating point representation
i) 0.640492×2^{-2} ii) -0.638454×2^5 .
Use 4 – bits to represent exponent and 12 – bits for mantissa. (07 Marks)

OR

- 10 a. With a neat diagram, explain the basic architecture of TMS320C54X family DS processors. (10 Marks)
- b. Describe the IEEE single precision floating point format used in DS processors. (05 Marks)
- c. Find the signed Q – 15 representation for the decimal number 0.560123. (05 Marks)