CBCS SCHEME

USN | | | | | | | | | | 18EC56

Fifth Semester B.E. Degree Examination, Jan./Feb. 2021
Verilog HDL

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the typical design flow for VLSI IC circuit using block diagram. **(08 Marks)**

b. Explain the trends in HDLs (Hardware Description Languages). **(04 Marks)**

c. Apply the bottom-up methodology to demonstrate the design of 4-bit ripple carry counter. **(08 Marks)**

OR

2 a. Define Module and Instance. Describe 4 different levels of abstractions used in Verilog HDL to describe target design. **(10 Marks)**

b. Explain top down design methodology and bottom up design methodology. **(10 Marks)**

Module-2

3 a. What are system tasks and compiler directives? Explain with example. **(08 Marks)**

b. Check the correctness of the following legal strings. If not, write the correct strings.
i) "This is a string displaying the % sign"
ii) "Out = in1 + in2"
iii) "Please ring a bell \ 007"
iv) "This is a backslash \ character \ n" **(04 Marks)**

c. Declare the following variables in verilog:
i) An 8-bit vector net called a_in
ii) A 32 bit storage register called address. Bit 31 must be in MSB. Set the value of the reg. to a 32 bit decimal number equal to 3.
iii) An integer called count
iv) A time variable called snap_shot
v) An array called delays, Array contains 20 elements of the type integer
vi) A memory MEM containing 256 words of 64 bits each
vii) A parameter cache-size equal to 512. **(08 Marks)**

OR

4 a. With a neat block diagram, explain the components of a verilog module by highlighting mandatory blocks. **(08 Marks)**

b. Explain the port connection rules of verilog HDL. **(08 Marks)**

c. A 4-bit parallel shift register has I/O pins as shown in Fig.Q.4(c) below. Write the module definition for this module shift_reg. Include the list of ports and port declaration. **(04 Marks)**

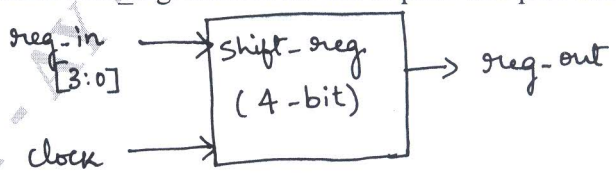

Fig.Q.4(c)

Module-3

5 a. Use gate level description of verilog HDL to design 4:1 MUX truth table, gate level block, logic expression and logic diagram. Write the stimulus block. **(10 Marks)**

b. Write gate level description to implement y = ab + c with 5 and 4 time units of gate delay for AND and OR gate respectively. Also write the stimulus block and simulation waveforms. **(10 Marks)**

OR

6 a. Write the dataflow modeling verilog code for 4-to-1 multiplexer using
i) Logic equation ii) Conditional operator. **(10 Marks)**

b. Explain assignment delay, implicit assignment delay and net declaration delay for continuous assignment statements with examples. **(04 Marks)**

c. Write a dataflow level verilog code using + and { } operators for 4-bit full adders. **(06 Marks)**

Module-4

7 a. Explain the blocking assignments and non-blocking assignment statements with relevant examples. **(08 Marks)**

b. Explain briefly the different types of event based timing control in verilog. **(08 Marks)**

c. Write a note on the following loop statements:
i) While loop ii) Forever loop. **(04 Marks)**

OR

8 a. Write a verilog behavioral code for 4 to 1 MUX using CASE statement. **(08 Marks)**

b. Explain the sequential and parallel blocks with examples. **(08 Marks)**

c. Define a function to multiple two 4-bit numbers 'a' and 'b'. The output is an 8 bit value. Invoke function by using stimulus and check results. **(04 Marks)**

Module-5

9 a. Write a note on:
i) Assign and deassign
ii) Overriding parameters. **(10 Marks)**

b. Create a design that uses the full adder. Use a conditional compilation ('if def.). Compile the fulladder 4 with def param statement if the text macro DPARAM is defined by the 'define statement; otherwise, compile the Fulladder4 with module instance parameter values. **(06 Marks)**

c. What will be the output of the $display statement shown below

```
Module TOP;
A a1( );
end module
Module A;
B b1( );
end module
Module B;
initial
$display {"I am inside instance % m"); end module.
```

(04 Marks)

OR

10 a. With a neat flow chart explain computer-aided logic synthesis process. **(10 Marks)**

b. Write RTL description for magnitude comparator. **(06 Marks)**

c. What is logic synthesis? **(04 Marks)**

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