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10EC56

Fifth Semester B.E. Degree Examination, Jan./Feb. 2021
Fundamentals of CMOS VLSI

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Derive CMOS inverter DC characteristics graphically and explain. **(08 Marks)**
b. Explain the mask sequence of CMOS P-well inverter with neat sketches. **(08 Marks)**
c. Briefly discuss pass transistor and tristate inverter. **(04 Marks)**

2 a. Draw symbolic form diagram of 1 bit CMOS shift register cell. **(06 Marks)**
b. What is stick diagram? Draw stick and layout diagram for $y = \overline{ABC + DE}$. **(08 Marks)**
c. Explain design rules for wires (nMOS and CMOS). **(06 Marks)**

3 a. Draw two input NAND gate using BiCMOS and CMOS domino logic. **(06 Marks)**
b. Explain with neat diagram, the drawback of dynamic CMOS logic and explain how above dronoback is eliminated using necessary diagram. **(08 Marks)**
c. Explain in detail simple CVSL. **(06 Marks)**

4 a. Explain the problem of driving large capacitive loads. **(08 Marks)**
b. Discuss the effect of scaling on gate capacitance maximum operating frequency, current density and power speed product. **(08 Marks)**
c. Define sheet resistance and standard unit of capacitance □cg. **(04 Marks)**

PART – B

5 a. Briefly discuss n-p CMOS logic. **(04 Marks)**
b. Design bus arbitraton logic for n-line bus. **(10 Marks)**
c. Discuss two-phase clock generator using D-flip flops. **(06 Marks)**

6 a. Explain basic bus architectures. **(06 Marks)**
b. With a neat diagram, explain the arrangement of an adder element for both arithmetic and logical functions. **(08 Marks)**
c. Explain carry select adder with neat structure. **(06 Marks)**

7 a. Explain JK flip-flop arrangement as static memory element. **(08 Marks)**
b. Explain pseudo static register cell. **(08 Marks)**
c. With a neat diagram, explain CMOS pseudo-static D-flip-flop. **(04 Marks)**

8 a. Draw a circuit model for inverter driving an inverter on a Δ% transition. **(04 Marks)**
b. Explain the requirement by the I/O pads. **(06 Marks)**
c. Write note on test and testability. **(10 Marks)**

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