CBCS SCHEME

USN | | | | | | | | | | 15EC655

# Sixth Semester B.E. Degree Examination, Jan./Feb. 2021
## Microelectronics

Time: 3 hrs. Max. Marks: 80

**Note:** ***Answer FIVE full questions, choosing ONE full question from each module.***



### Module-1

1 a. Derive an expression for drain current of NMOS transistor operating in different regions. **(08 Marks)**

b. Calculate the minimum value of $V_{DS}$ needed for a 0.8μm process technology for which $t_{ox} = 15nm$, $\mu_n = 550cm^2/V.S$.

i) Find $C_{ox}$, $K_n^1$

ii) Find the over drive voltage required to operate the transistor having (W/L) = 20 in saturation with $I_D = 0.2mA$. **(08 Marks)**

**OR**

2 a. Analyse the circuit in Fig.Q2(a) to determine all voltage and currents. Let :

$V_t = 1V$, $K_n^1\left(\frac{W}{L}\right) = 1mA/v^2$.

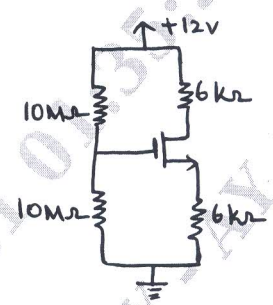


Fig.Q2(a) **(08 Marks)**

b. Derive an expression for resistance between drain and source from the transfer characteristics. **(08 Marks)**

### Module-2

3 a. Derive an expression for MOSFET transconductance using small signal operation. **(08 Marks)**

b. Differentiate between small signal equivalent model and T-equivalent model of MOSFET. **(08 Marks)**

**OR**

4 a. Derive an expression for $R_{in}$, $R_0$ gain for a grounded gate amplifier. Justify why it is called as current followers. **(08 Marks)**

b. Briefly explain all the capacitances in MOSFET and draw its high frequency model. **(08 Marks)**

## Module-3

5 a. Compare MOSFET and BJT based on the following parameters.
   i) Current – voltage equation
   ii) Hybrid-π model
   iii) Transition frequency
   iv) Gain. **(08 Marks)**

   b. Draw the MOSFET constant current source and explain its operation. **(04 Marks)**

   c. For $V_{DD} = 3V$, $I_{ref} = 100\mu A$ design a constant current source if $Q_1$ and $Q_2$ are matched and have a channel length of $1\mu m$, channel width of $10\mu m$, $V_t = 0.7V$, $K_n^1 = 200\mu A.V^2$. **(04 Marks)**

**OR**

6 a. Explain MOS current steering circuits with relevant current-voltage equations. **(08 Marks)**

   b. Find the value of Z for the circuit shown in Fig.Q6(b) using Miller equivalent circuit when Z is : i) 1 – MΩ resistance ii) 1 – pF capacitance.

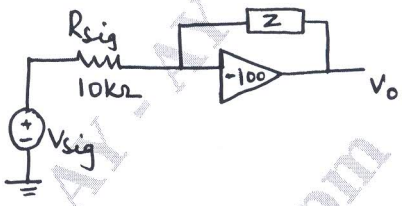


Fig.Q6(b) **(08 Marks)**

## Module-4

7 a. Derive the 3-dB frequency expression for a common source amplifier. **(08 Marks)**

   b. A CMOS common source amplifier has $\left(W/L\right) = \frac{7.2\mu m}{0.36\mu m}$ for all transistors,

   $\mu_n Co_x = 387\mu A/v^2$, $\mu_p Co_x = 86\mu A/v^2$, $I_{ref} = 100\mu A$, $V_A = 5V/\mu m$, $C_{gs} = 20fF$, $C_{gd} = 5fF$, $C_L = 25fF$, $R_{sig} = 10K\Omega$, determine $F_H$. **(08 Marks)**

**OR**

8 a. Explain an active loaded common gate amplifier and derive for its $R_{in}$, $R_0$, gain. **(08 Marks)**

   b. Estimate $A_{vo}$, $R_{in}$, $R_0$, $G_v$, $F_H$ for a common gate amplifier with $\left(W/L\right) = \frac{7.2\mu m}{0.36\mu m}$,

   $\mu nC_{ox} = 387\mu A/v^2$, $r_0 = 18k\Omega$, $I_D = 100\mu A$, $g_m = 1.25mA/v$, $X = 0.2$, $R_S = 10k\Omega$, $R_L = 100k\Omega$, $C_{gs} = 20fF$, $C_{gd} = 5fF$, $C_L = 0$. **(08 Marks)**

## Module-5

9 a. Explain the MOS differential pair operation with common mode and differential input voltage. **(08 Marks)**

   b. Explain the effect of $R_D$ and $g_m$ mismatch on CMRR. **(08 Marks)**

**OR**

10 a. Determine the differential gain of an active loaded MOS pair. **(08 Marks)**

   b. With a neat circuit diagram, explain the operation of two stage CMOS opamp configuration. **(08 Marks)**

* * * * *