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10EC751

Seventh Semester B.E. Degree Examination, Jan./Feb. 2021
DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Explain the process of decimation and interpolation with block diagrams. **(08 Marks)**

b. The signal sequence x(n) = [0, 4, 8, 12, 16] is interpolated using the interpolation sequence $b_k = \left[\frac{1}{4}, \frac{2}{4}, \frac{3}{4}, 1, \frac{3}{4}, \frac{2}{4}, \frac{1}{4}\right]$ and the interpolation factor is 4. Find the interpolated sequence y(m). **(08 Marks)**

c. An analog signal is sampled at a sampling rate of 8 KHz. If 512 samples of this signal are used to compute DFT, i.e., X(K), determine the frequency spacing between adjacent X(K) elements. Determine the analog frequency corresponding to K = 64, 128 and 200. **(04 Marks)**

2 a. Draw and explain 3 × 3 braces multiplier structure for unsigned integers. **(08 Marks)**

b. Identify the addressing modes of the operands in each of the following instruction and their operations. i) ADD B ii) ADD # 1234h iii) ADD 2233h iv) ADD * addrreg, offsetreg +. **(04 Marks)**

c. Discuss the features of address generation unit of a programmable DSP with the help of a diagram. **(08 Marks)**

3 a. Explain the operation of direct addressing made of TMS320C54XX processor with a diagram. **(07 Marks)**

b. Assuming the contents of AR3 to be 200h, what will be its contents after each of the following TMS320C54XX addressing modes is used? Assume that the contents of AR0 are 20h. i) *AR3 + 0 ii) *AR3 – 0 iii) *AR3 –
iv) *+AR3(40h) v) *+AR3(–40h) vi) *AR3 + OB. **(06 Marks)**

c. Discuss the features of program control unit of TMS320C54XX processor. **(07 Marks)**

4 a. Describe the operation of the following instructions :
i) MAC *AR2 –, *AR4+, B, A
ii) ADD # 2345h, –4, B, A
iii) MPY *AR3–, *AR4 + 0, B **(06 Marks)**

b. With the help of figure, explain the pipeline operation of the following sequence of instruction of the initial values of AR1, AR3, A are 104, 101, 2 and the values stored in memory locating 101, 102, 103, 104 are 4, 6, 8 12 (decimal value). Also provide the values of registers AR3, AR1, T and accumulator A and B after completion of each cycle.

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ADD  *AR3+, A
LD   *AR1+, T
MPY  *AR3+, B
ADD   B, A
  – – –
  – –– 
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(08 Marks)

c. Describe the hardware timer on chip peripheral of TMS320C54XX processor with a block diagram. **(06 Marks)**

PART – B

5 a. Explain the significance of Q – notation in DSP. **(04 Marks)**
b. What values are represented by 16 bit numbers :
i) N = 4400h as Q15 notation
ii) N = 5736h as Q6 notation
iii) N = 3000h as Q12 notation. **(06 Marks)**
c. Explain the implementation of digital interpolation using FIR filter and poly-phase filter. **(10 Marks)**

6 a. Explain a general DIT FFT butterfly inplace computation structure. Also explain how scaling prevents overflow condition in the butterfly computation. **(12 Marks)**
b. Explain the bit reversed index generation for 8 point DIT FFT. **(05 Marks)**
c. Determine the following for a 256 point FFT computation :
i) Number of stages
ii) Number of butterflies in each stage
iii) Number of butterflies need for the entire computation. **(03 Marks)**

7 a. Explain the memory space of TMS320C54XX processor. **(04 Marks)**
b. Design a data memory system with address range 000800h – 000FFFh for a C5416 processor using 2K × 8 SRAM memory chips. **(08 Marks)**
c. Discuss the interrupt handling by the TMS320C54XX processor with the help of flow chart. **(08 Marks)**

8 a. Describe the PCM 3002 CODEC with the help of a block diagram. **(08 Marks)**
b. Explain encoding and decoding of JPEG image processing system using TMS320C54XX with relevant block diagrams. **(12 Marks)**

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