CBCS SCHEME

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17MT35

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define filter. Give the classification of filters. Mention the advantages of Active filter over passive filter. Plot the frequency response of major active filters. **(12 Marks)**

b. With the neat circuit diagram derive the expression for gain of HPF, also plot the frequency response curve. **(08 Marks)**

OR

2 a. Design a low pass filter at a cutoff frequency of 1KHz with a passband gain of 2. Using the frequency scaling technique, convert 1KHz cutoff frequency of 1.6KHz. **(10 Marks)**

b. With the neat sketch, explain the operation of All pass filters. Mention its application in the communication system. Also derive the expression for gain. For the all pass filter with f_{in} =1KHz and R = 1.5kΩ and c = 0.01μF, find the phase angle ϕ. **(10 Marks)**

Module-2

3 a. Define Oscillator, with the neat block diagram, explain the principle of Oscillation. **(08 Marks)**

b. With the neat sketch and relevant equations, explain the working of RC-phase shift oscillator circuit. Also design a RC phase shift oscillator with f_0 = 200Hz **(12 Marks)**

OR

4 a. With the neat sketch and waveforms, explain the operation of Noninverting comparator circuit. **(10 Marks)**

b. Explain how Inverting comparator circuit can be used as Schmitt trigger. **(10 Marks)**

Module-3

5 a. Explain how 555 timer can be used as mono-stable multivibrator with neat block diagram. **(10 Marks)**

b. Explain how mono-stable multivibrator can be used as divide by 2 network. Also Design a mono-stable multivibrator as divide by 2 network with the input frequency of 2KHz and c = 0.01μF. **(10 Marks)**

OR

6 Explain Astable Multivibrator application as
i) Square wave oscillator
ii) Free running ramp generator. **(20 Marks)**

Module-4

7 a. Simply the following Boolean function in i) Sum of products ii) Product of sums
$F = (A, B, C, D) = \varepsilon (0, 1, 2, 5, 8, 9, 10)$ **(10 Marks)**

b. Implement a Half adder circuit and also implement a Full adder circuit using two half adders. **(10 Marks)**

OR

8 a. Define Multiplexer. Construct a 4:1 MUX using basic gates. **(06 Marks)**

b. Design a Full adder circuit using MUX. **(08 Marks)**

c. Implement a 4 × 16 decoder using two 3 × 8 decoder. **(06 Marks)**

Module-5

9 a. With a neat circuit diagram and truth table derive the characteristic equation for i) Clocked SR Flip-Flop ii) Clocked J K Filp-Flop. **(12 Marks)**

b. Design a 3 bit binary ripple up counter. **(08 Marks)**

OR

10 a. Design a BCD ripple counter using JK flip-flop. **(10 Marks)**

b. Design a Synchronous 3 bit up counter. **(10 Marks)**

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