CBCS SCHEME

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Analog and Digital Electronics

Time: 3 hrs.   Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1   a.   Define clamper circuit. Explain the positive clamper circuits with output waveforms.
                                                                              (05 Marks)

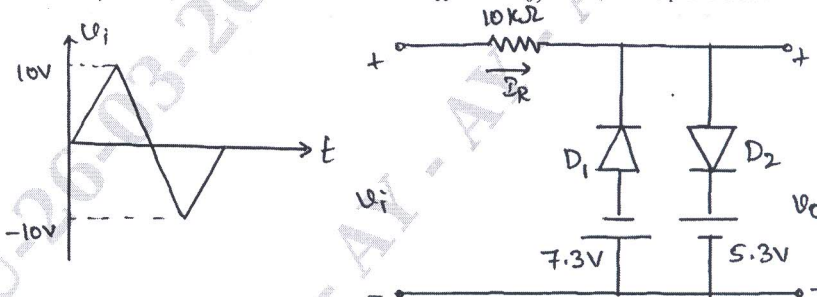   b.   For the circuit shown, sketch the waveforms of i_R and v_0, assume S_i diodes.   **(07 Marks)**

Fig. Q1 (b)

   c.   Explain the operation of RC coupled BJT amplifier.   **(08 Marks)**

OR

2   a.   Explain the operation of second order High pass butterworth filter and draw its frequency response.   **(10 Marks)**

   b.   Design a wide band-pass filter with $f_L = 200$ Hz and $f_H = 1$ kHz and a passband gain = 4. Draw the frequency response plot and calculate the value of 'Q' for the filter.   **(10 Marks)**

Module-2

3   a.   With a neat circuit diagram, explain wein bridge oscillator.   **(10 Marks)**
   b.   Design the phase shift oscillator for frequency of oscillation, $f_0 = 200$ Hz.   **(05 Marks)**
   c.   What is frequency stability? Explain its significance.   **(05 Marks)**

OR

4   a.   Define Comparator. Explain the operation of inverting comparator.   **(10 Marks)**
   b.   With the help of input and output waveforms. Explain the operation of Schmitt trigger circuit.   **(10 Marks)**

Module-3

5   a.   Explain the operation of 555 timer as monostable multivibrator and derive the expression for pulse width.   **(10 Marks)**
   b.   Design a 555 astable multivibrator for an output frequency of 1 kHz and duty cycle 60%.
                                                                              (10 Marks)

OR

6   a.   With a neat sketch, explain the architecture of 555 Timer.   **(06 Marks)**
   b.   List out the features and applications of 555 Timer.   **(06 Marks)**
   c.   Derive an expression for charging time (T_C) discharging time (T_d) frequency of oscillation and duty cycle for a astable multivibrator for 555 timer.   **(08 Marks)**

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Module-4

7 a. State the rules for K-map simplification. **(04 Marks)**

   b. Simplify the following switching function using K-map:

   $F(A,B,C,D) = \sum (0, 5, 7, 8, 9, 10, 11, 14, 15) + \phi(1, 4, 13)$ **(06 Marks)**

   c. Explain the working of 8×1 MUX with operation table and logic diagram using 4 : 1 MUX. **(10 Marks)**

OR

8 a. Explain the full subtractor circuit with a truth table and logic diagram. **(10 Marks)**

   b. What is Encoder? Realize Octal to binary Encoder using basic gates and write its truth table. **(10 Marks)**

Module-5

9 a. Explain clocked D flip-flop with the following :
   (i) Logic diagram.
   (ii) Truth table.
   (iii) Input and Output waveform. **(10 Marks)**

   b. Discuss BCD ripple counter using JK flip flop with state diagram, logic diagram and timing diagram. **(10 Marks)**

OR

10 a. Explain clocked JK flip flop by the following:
   (i) Logic diagram.
   (ii) Characteristic table.
   (iii) Characteristic equation. **(10 Marks)**

   b. Draw and explain the working of 4-bit up synchronous counter. **(10 Marks)**

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