CBCS SCHEME

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15EE35

Third Semester B.E. Degree Examination, July/August 2021
Digital System Design

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions.***

1 a. Express the following equations into proper canonical forms and in decimal notations
   i) $F_1(a, b, c) = a\bar{b} + a\bar{c} + bc$
   ii) $f_2(A, B, C) = \bar{A}\bar{B} + C$. **(06 Marks)**

b. Simply the following equations using K Map and implement using logic gates
   i) $f(a, b, c, d) = \pi M(0, 3, 4, 7, 8, 10, 12, 14) + d(2, 6)$
   ii) $f(w, x, y, z) = \Sigma m(0, 2, 8, 10, 11, 12, 14, 15)$ **(10 Marks)**

2 a. Simplify using Quine Mc Cluskey method.
   $P = f(a, b, c, d) = \Sigma m(2, 3, 4, 5, 13, 15) + \Sigma(8, 9, 10, 11)$. **(10 Marks)**

b. Solve using 3 variable MEV Kmap with d as MEV.
   $f(a, b, c, d) = \Sigma m(0, 1, 3, 5, 6, 11, 13) + d(4, 7)$. **(06 Marks)**

3 a. What is a magnitude comparator? Design a 2 bit binary comparator. **(10 Marks)**

b. Realize the following function using 8:1MUX with a, b, c as select lines
   $f(a, b, c, d) = \Sigma m(0, 1, 5, 6, 7, 9, 10, 15)$ **(06 Marks)**

4 a. Write the function table and draw the interfacing diagram of ten key keypad interfaces to a digital system using decimal to BCD encoder. **(08 Marks)**

b. Using active high output 3:8 line decoder, implement the following functions.
   $F_1(A, B, C, D) = \Sigma m(0, 1, 2, 5, 7, 11, 15)$ and $f_2 = (A, B, C, D) = \pi(3, 7, 9, 13)$. **(08 Marks)**

5 a. Explain the working of Master Slave JK flip-flop with the help of logic diagram, function table, logic symbol and timing diagram. **(10 Marks)**

b. Obtain the characteristics equation of JK flip-flop and T flip-flop. **(06 Marks)**

6 a. Design a synchronous Mod 6 counter using JK flip-flop. **(08 Marks)**

b. Design a 4bit register using positive edge triggered DFF to operate as indicated in the table below.

Mode	Select	Register
a_1	a_0	Operation
0	0	Hold
0	1	Clear
1	0	Complement
1	1	Circular right shift

(08 Marks)

7 a. Compare Mealy and Moore models of a clocked synchronous sequential circuit. **(04 Marks)**

b. Construct the excitation table, transition table and state diagram for the Moore sequential logic circuit given below in Fig Q7(b).

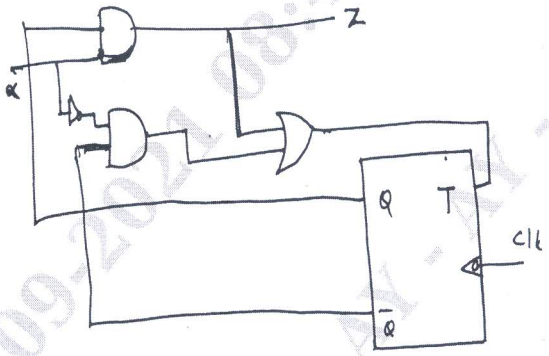

Fig Q7(b) **(12 Marks)**

8 a. Construct a sequential logic circuit single input single output by obtaining the state and excitation table for the given diagram using JK flip – flop. (Ref. Q8(a)

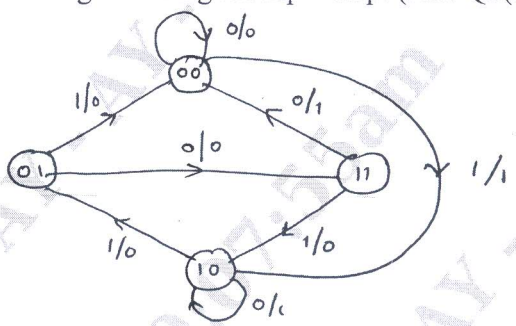

Fig Q8(a) **(10 Marks)**

b. Draw the state diagram for a sequence detector to detect the sequence 110. **(06 Marks)**

9 a. Explain the structure of VHDL module and verilog module with an example of half adder. **(08 Marks)**

b. Explain shift operators of VHDL and verilog with an example of 4bit vector 1101. **(08 Marks)**

10 a. Draw the block diagram of a 4bit look ahead carry adder and write the data flow description for its boolean functions in verilog. **(08 Marks)**

b. Draw the logic diagram, of a D latch and write the VHDL code description. **(08 Marks)**

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