



# CBCS SCHEME

18EE46

## Fourth Semester B.E. Degree Examination, July/August 2021 Operational Amplifiers and Linear IC's

Time: 3 hrs.

Max. Marks: 100

**Note: Answer any FIVE full questions.**

- 1 a. Explain block diagram representation of a typical op-amp. (08 Marks)  
b. Explain open loop op-amp configurations. (12 Marks)
- 2 a. Explain electrical characteristics of an ideal op-amp. (08 Marks)  
b. Explain summing, scaling and averaging of an inverting amplifier. (12 Marks)
- 3 a. With neat diagram, explain first order low pass Butterworth filter. (10 Marks)  
b. Design a wide band pass filter with  $f_L = 200\text{Hz}$ ,  $f_H = 1\text{KHz}$  and a pass band gain = 4. Draw the frequency response of the filter and calculate the Q for the filter. (10 Marks)
- 4 a. Explain voltage follower regulator. (10 Marks)  
b. Explain integrated circuits regulator. (10 Marks)
- 5 a. Explain triangulation /rectangular wave generation. (12 Marks)  
b. Explain RC phase shift oscillators. (08 Marks)
- 6 a. With neat diagram, explain inverting Schmitt trigger circuit. (10 Marks)  
b. Explain voltage-frequency converter. (10 Marks)
- 7 a. Explain R-2R D/A converter. (10 Marks)  
b. Explain full wave precision rectifier. (10 Marks)
- 8 a. Explain successive approximation ADC. (10 Marks)  
b. Explain integrated circuit 8 bit D/A converter. (10 Marks)
- 9 a. Explain phase locked loop. (10 Marks)  
b. Briefly explain performance factors of PLL. (10 Marks)
- 10 a. Explain internal architecture of 555 timer. (10 Marks)  
b. Explain Monostable multivibration. (10 Marks)

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Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
2. Any revealing of identification, appeal to evaluator and /or equations written eg,  $42+8 = 50$ , will be treated as malpractice.