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15MT62

Sixth Semester B.E. Degree Examination, July/August 2021
Embedded Systems (ARM)

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions.

1 a. Explain the RISC design philosophy in detail. **(08 Marks)**
   b. Discuss the memory and peripheral concept in Embedded system hardware. **(08 Marks)**

2 a. Explain Core Extension with neat diagram. **(08 Marks)**
   b. Describe pipeline concept in detail. **(08 Marks)**

3 a. Explain the barrel shifter operation using data processing instruction. **(08 Marks)**
   b. Explain the branch instruction with syntax and example. **(08 Marks)**

4 a. Write the variation of STRH instruction. **(04 Marks)**
   b. Write addressing mode for load store multiple instructions. **(04 Marks)**
   c. Explain
      i) Thumb Register Usage
      ii) ARM Thumb interworking. **(08 Marks)**

5 a. Explain Load scheduling concept by unrolling to the str to lower function. **(08 Marks)**
   b. Discuss the most of available Register with Example. **(08 Marks)**

6 a. Explain conditional Execution concept with example. **(08 Marks)**
   b. Write Decremented counted looping in looping constructs. **(08 Marks)**

7 a. Explain the cache polices concept in detail. **(08 Marks)**
   b. With neat diagram, explain the relationship of cache has between the processor core and main memory. **(08 Marks)**

8 Describe the following concept in cache lockdown.
      i) Locking a cache by incrementing the way index
      ii) Locking a cache using lock bits. **(16 Marks)**

9 Explain the following exception handling concepts.
      i)   Vector table **(04 Marks)**
      ii) Exception priorities **(04 Marks)**
      iii) Link Register offset **(08 Marks)**

10 Explain following interrupt handler
      i) Non nested interrupt handler **(08 Marks)**
      ii) Priority interrupt handler. **(08 Marks)**

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