CBCS SCHEME

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15EE34

Third Semester B.E. Degree Examination, Feb./Mar. 2022
Analog Electronic Circuits

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Draw and explain series negative clipper with the help of output waveform and transfer characteristics. **(04 Marks)**

b. Derive an expression for $S(iC_O)$ and $S(V_{BE})$ for fixed bias. **(06 Marks)**

c. Determine the following for the fixed-bias configuration of Fig.Q1(c).
(i) I_{BQ} and I_{CQ} (ii) V_{CEQ} (iii) V_B and V_C

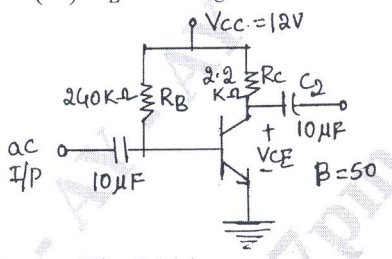


Fig.Q1(c) **(06 Marks)**

OR

2 a. Explain Emitter bias circuit, with the help of BE loop and CE loop. Write necessary equation. **(08 Marks)**

b. Design a suitable circuit represented by the box shown in Fig.Q2(b), which had input and output waveforms as indicated.

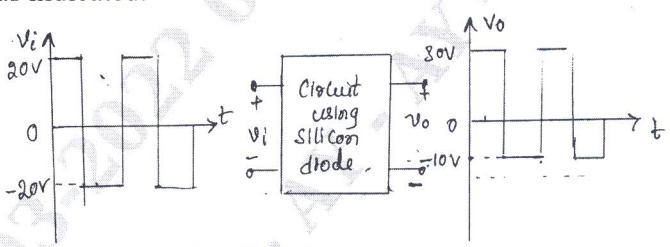
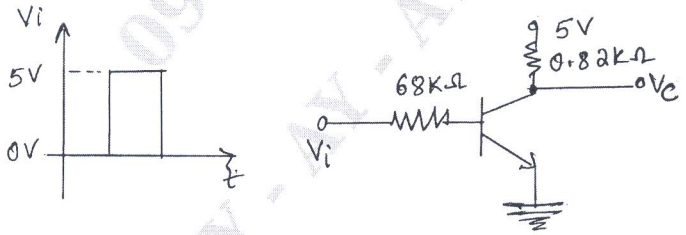


Fig.Q2(b) **(04 Marks)**

c. Fig.Q2(c) shows the transistor switch check whether the circuit works properly.



$V_{CE} = 0.7V$
$VCE(SAT) = 0.15V$
$I_{CEO} = 10\ \mu A$
$\beta_{dc} = h_{FE} = 125$

Fig.Q2(c) **(04 Marks)**

Module-2

3 a. Define h-parameters. Hence derive h-parameter model of a CE – BJT. **(06 Marks)**

b. For the common base configuration of Fig.Q3(b). $I_E = 4$ mA, $\alpha = 0.991$. An ac signal of 3 mV is applied between the base and emitter terminals. If $R_L = 610\ \Omega$. Calculate
(i) r_v and z_i (ii) A_v and A_i

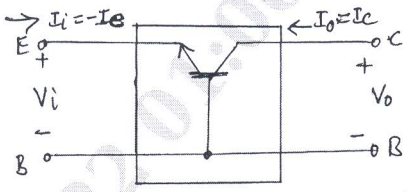


Fig.Q3(b) **(04 Marks)**

c. For the circuit shown in Fig.Q3(c),
(i) Determine r_e (ii) Find z_i, z_o, A_v and A_i (with $r_o = \infty\ \Omega$)

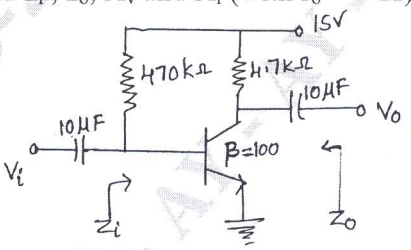


Fig.Q3(c) **(06 Marks)**

OR

4 a. Draw the emitter follower circuit. Derive expression for (i) z_i (ii) z_o (iii) A_v using re model. **(08 Marks)**

b. Derive the expressions for Miller's effect capacitance. **(08 Marks)**

Module-3

5 a. Explain the need of cascading amplifier? Draw and explain the block diagram of two stage cascade amplifier. **(06 Marks)**

b. For the amplifier circuit shown in Fig.Q5(b), calculate z_i, z_o, A_i and A_v.

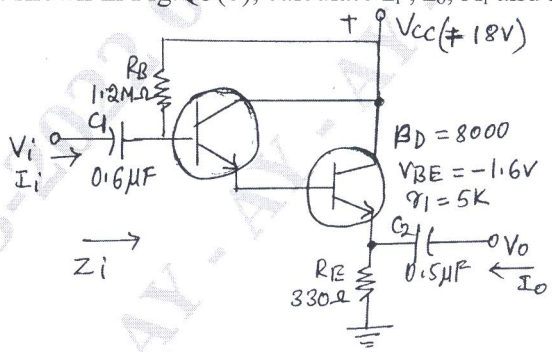


Fig.Q5(b) **(04 Marks)**

c. Derive the expression for input resistance (R_{if}) for a current series feedback. **(06 Marks)**

OR

6 a. With necessary equivalent diagram, obtain the expression for z_{in}, A_v, z_o for a Darlington Emitter follower. **(10 Marks)**

b. An amplifier with open loop voltage gain of 1000 deliver 10W of power output at 10% second harmonic distortion when i/p is 10 mV. If 40 dB negative feedback is applied and output power is to remain at 10W, determine required input signal V_s and second harmonic distortion with feedback. **(06 Marks)**

Module-4

7 a. Show that series fed directly coupled class A power amplifiers has a maximum power efficiency of 25%. **(10 Marks)**

b. With a neat diagram, Explain the working of R-C phase shift oscillator. **(06 Marks)**

OR

8 a. Compare RC phase shift oscillator with wein bridge oscillator. **(04 Marks)**

b. The following data are available for the Colpitts oscillator.

$C_1 = 1$ nF, $C_2 = 99$ nF, $L = 1.5$ mH

$L_{RFC} = 0.5$ mH $C_c = 10$ μF, $h_{fc} = 110$

(i) Calculate the frequency of oscillation

(ii) Check to make sure that the condition for oscillation is satisfied. **(06 Marks)**

c. Calculate the peak power dissipated in each transistor of a class B, push pull power amplifier if $V_{CC} = 15$V and $R'_L = 5\Omega$. **(06 Marks)**

Module-5

9 a. Draw JFET amplifier using fixed bias configuration. Derive z_i , z_o , A_v for small signal model. **(10 Marks)**

b. For the JFET amplifier shown in Fig.Q9(b).

(i) Calculate z_i and z_o (ii) Calculate A_v (iii) Find V_o if $V_i = 25$mV(rms)

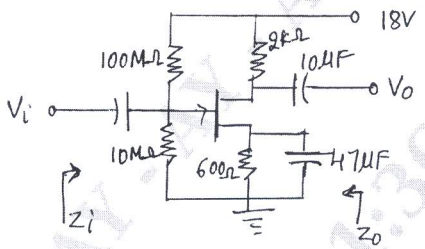


Fig.Q9(b)

$I_{DSS} = 12$ mA
$V_p = -3$V
$V_{os} = 10$ μs
$V_{GSQ} = -1$V

(06 Marks)

OR

10 a. Explain the structure of the Depletion mode MOSFET. **(08 Marks)**

b. Define Transconductance g_m . Derive an expression for g_m . **(04 Marks)**

c. List the difference between FET and BJT. **(04 Marks)**

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