

Fourth Semester B.E. Degree Examination, July/August 2021 Operational Amplifiers and Linear ICs

Time: 3 hrs.

Max. Marks: 100

**Note:1. Answer any FIVE full questions.
2. Any missing data may be assumed suitably.**

1. a. What is an op-amp? Explain the block diagram representation of a typical op-amp. (08 Marks)
b. Define the following electrical parameter as,
(i) Input offset voltage
(ii) CMRR
(iii) Slew rate. (06 Marks)
c. Briefly explain the difference between the dc and ac amplifier with a suitable circuit. (06 Marks)
2. a. What are the characteristics of an ideal op-amp? (04 Marks)
b. What is an instrumentation amplifier? Explain the instrumentational amplifier using transducer bridge resistance. Obtain the output voltage in terms of changing in resistance of the transducer. (10 Marks)
c. Explain the summing amplifier in any mode operation. Show that output voltage of a summing is equal to $\frac{1}{3}$ of all input voltages. (06 Marks)
3. a. Define an active filters. Explain the first order low pass butter worth filter with a frequency response. (06 Marks)
b. Design a single stage band pass filter to have unity voltage gain and a pass band from 300 Hz to 30 Hz. (08 Marks)
c. Explain the following terms referred to the voltage regulator (i) line regulation (ii) Load regulation and Ripple rejection. (06 Marks)
4. a. What are the advantages of an active filler over passive filter? (04 Marks)
b. Sketch the circuit of a voltage follower regulator using op-amps. Explain the circuit operation. (08 Marks)
c. Using LM317 ICs, design an adjustable voltage regulator to satisfy the following specifications:
Output voltage $V_0 = 5$ to 12 volt
Input current $I_0 = 1.0$ Amp
(Assume $I_{ADJ} = 100 \mu A$, $V_{ref} = 1.25$ volt) (08 Marks)
5. a. Sketch the circuit of a triangular / rectangular waveform generator. Draw the output waveforms and explain the circuit operation. (08 Marks)
b. Design a phase shift oscillator to have an output of 3.5 KHz. Use 741 IC op-amp with supply voltage of $\pm 12V$. (07 Marks)
c. Draw the circuit diagram for an op-amp inverting zero cross detector with waveforms and explain its operation. (05 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

- 6 a. Use a 741 IC op-amp, design an inverting Schmitt trigger circuit to trigger at $\pm 2V$ input and produce a $\pm 11 V$ output. (08 Marks)
b. Draw and explain the working voltage to current converter with grounded load. (06 Marks)
c. Draw a neat diagram and explain the operation of an inverting Schmitt trigger circuit. Draw its hysteresis curve. (06 Marks)
- 7 a. Design a nonsaturating precision half wave rectifier to produce a 2 V peak output from a 1 MHz sinewave input a 0.5 V peak value. Use a bipolar op-amp with a supply voltage of $\pm 15V$. (06 Marks)
b. With a neat circuit diagram, explain precision full wave rectifier as combination of a summing circuit and half wave rectifier. Draw the input and output waveform. (08 Marks)
c. Draw the block diagram and waveform for a linear ramp type ADC. Explain its operation with waveforms. (06 Marks)
- 8 a. Discuss the advantage of a precision rectifier over an ordinary diode rectifier. (04 Marks)
b. With a neat circuit diagram, explain the working of 3 bit R-2R DAC. Draw a output versus inputs. (08 Marks)
c. Draw a neat block diagram of the successive-approximation type ADC. (08 Marks)
- 9 a. Draw the block diagram and waveform for a PLL (Phase-Locked Loop) system. Explain its function. (06 Marks)
b. Draw and explain the functional block diagram of a 555 timer for each component parts. (08 Marks)
c. Briefly explain the roles of a low pass filter and VCO in PLLs. (06 Marks)
- 10 a. Using the 555 timer, design a monostable multivibrator an output pulse width of 100 ms. (08 Marks)
b. Explain the working of the monostable multivibrator as a pulse stretcher using 555 ICs. (06 Marks)
c. Write a short notes on : (i) Phase detector (ii) PLL performance factors. (06 Marks)
