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18EC52

Fifth Semester B.E. Degree Examination, Feb./Mar.2022

Digital Signal Processing

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Prove that the sampling of DTFT of a sequence $x(n)$ result in N-point DFT with a neat diagram. (10 Marks)
- b. Find the 4-point DFT of the sequence $x(n) = \{1, 0, 0, 1\}$ using matrix method and verify the answer by taking the 4-point IDFT of the result. (10 Marks)

OR

- 2 a. Derive the circular Time shift property. (06 Marks)
- b. Compute the circular convolution of the following sequences using DFT and IDFT method $x_1(n) = \{1, 2, 3, 4\}$ and $x_2(n) = \{4, 3, 2, 1\}$. (09 Marks)
- c. If $W(n) = \frac{1}{2} + \frac{1}{2} \cos\left[\frac{2\pi}{N}\left(n - \frac{N}{2}\right)\right]$, what is the DFT of the window sequence $y(n) = x(n).w(n)$? Relate the answer in terms of $X(K)$. (05 Marks)

Module-2

- 3 a. Find the output $y(n)$ of a filter whose impulse response is $h(n) = \{1, 1, 1\}$ and the input signal $x(n) = \{3, -1, 0, 1, 3, 2, 0, 1, 2, 1\}$ using overlap-add method. Assume the length of each block N is 6. (10 Marks)
- b. What do you mean by computational complexity? Compare the direct computation and FFT algorithms. In the direct computation of 32-point DFT of $x(n)$, How many
 - (i) Complex multiplications
 - (ii) Complex additions.
 - (iii) Real multiplications.
 - (iv) Real additions and
 - (v) Trigonometric function evaluations are required. (10 Marks)

OR

- 4 a. Develop 8-point DIT-FFT Radix-2 algorithm and draw the signal flow graph. (10 Marks)
- b. Given $x(n) = n + 1$ for $0 \leq n \leq 7$. Find $X(K)$ using DIF-FFT algorithm. (10 Marks)

Module-3

- 5 a. What are the different design techniques available for the FIR filters? Explain Gibbs phenomenon. Explain the four window techniques for the designing of FIR filters. (10 Marks)
- b. A low pass filter is to be designed with the following desired frequency response,

$$H_d(e^{j\omega}) = \begin{cases} e^{-j3\omega}, & \text{for } -\frac{3\pi}{4} \leq \omega \leq \frac{3\pi}{4} \\ 0, & \frac{3\pi}{4} \leq \omega \leq \pi \end{cases}$$

Determine $H(e^{j\omega})$ for $M = 7$ using Hamming window. (10 Marks)

OR

- 6 a. A FIR filter is given by,

$$y(n) = x(n) + \frac{2}{5}x(n-1) + \frac{3}{4}x(n-2) + \frac{1}{3}x(n-3)$$

Draw the lattice structure. (10 Marks)

- b. Based on the frequency-sampling method, determine the coefficients of a linear-phase FIR filter of length $M = 15$ which has a symmetric unit sample response and a frequency response that satisfies the conditions.

$$H\left(\frac{2\pi}{15}K\right) = 1; \quad K = 0, 1, 2, 3$$

$$= 0.4; \quad K = 4$$

$$= 0; \quad K = 5, 6, 7$$

(10 Marks)

Module-4

- 7 a. The normalized transfer function of a 2nd order Butterworth filter is given by,

$$H_2(S) = \frac{1}{S^2 + 1.414S + 1}$$

Convert the analog filter into digital filter with cut-off frequency of 0.5π rad/sec using bilinear transformation. Assume $T = 1$ sec. (10 Marks)

- b. A filter is given by the difference equation $y(n) - \frac{1}{4}y(n-1) + \frac{1}{8}y(n-2) = x(n) + \frac{1}{2}x(n-2)$.

Draw direct form - I and direct form - II realizations. Also obtain the transfer function of the filter. (10 Marks)

OR

- 8 a. Derive mapping function used in transforming analog filter to digital filter by bilinear transformation, preserves the frequency selectivity and stability properties of analog filter. (10 Marks)

- b. Design an IIR digital Butterworth filter that when used in the analog to digital with digital to analog will satisfy the following equivalent specification.

- (i) Low pass filter with -1 dB cut off 100π rad/sec.
- (ii) Stop band attenuation of 35 dB at 1000π rad/sec.
- (iii) Monotonic in stop band and pass band.
- (iv) Sampling rate of 2000 rad/sec.
- (v) Use bilinear transformation.

(10 Marks)

Module-5

- 9 a. With the block diagram, explain Digital Signal processors based on the Harvard architecture. (10 Marks)

- b. Discuss briefly the following special digital signal processor hardware units:

- (i) Multiplier and Accumulator (MAC) unit.
- (ii) Shifters.
- (iii) Address Generators.

(10 Marks)

OR

- 10 a. Discuss the following IEEE Floating-point formats:

- (i) Single precision format.
- (ii) Double precision format.

(10 Marks)

- b. With the diagram, explain the basic architecture of TMS320C54X family processor. (10 Marks)

(10 Marks)
