



OR

- 6 a. Implement 4-bit carry look ahead adder using Multiple Output Domino Logic (MODL) with necessary equations. (08 Marks)
- b. With neat circuit diagram and truth table, explain the operation of Manchester carry chain adder. (08 Marks)

**Module-4**

- 7 a. Explain the operation of  $(n + 1)$  bit parity generator with relevant circuit diagram and stick diagram. (08 Marks)
- b. Implement 4 : 1 MUX using switch logic with relevant truth table and equations. Also write the stick diagram. (08 Marks)

OR

- 8 a. With neat diagram, explain design abstraction for FPGA (Filed Programmable Gate Array). (08 Marks)
- b. Explain the architecture of field programmable gate array. (08 Marks)

**Module-5**

- 9 a. Explain the operation of 4 transistor dynamic memory and 6 transistor CMOS memory cells with sense amplifier circuit with neat circuit diagrams. (10 Marks)
- b. Explain the operation of D-latch using nMOS and CMOS design styles. (06 Marks)

OR

- 10 a. Identify various fault models and explain each fault model with relevant diagrams and layout. (12 Marks)
- b. Explain the operation of built in logic block observation (BILBO) used in testing. (04 Marks)

\*\*\*\*\*