

USN

--	--	--	--	--	--	--	--	--	--

Third Semester B.E. Degree Examination, Feb./Mar.2022
Computer Organization

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Explain the basic operational concepts of a computer, with a neat block diagram. (08 Marks)
- b. Explain basic input/output operations and write a program snippet to read a character and print it on screen till newline is encountered. (08 Marks)
- c. A program contains 1000 instructions, out of that 25% instructions requires 4 clock cycles, 40% instructions require 5 clock cycles and remaining requires 3 clock cycles for execution. Find the total time required to execute the program running in a 1 GHz machine. (04 Marks)

OR

- 2 a. What are addressing modes? Explain the following addressing modes, with an example for each, (i) Indirect mode (ii) Index mode (iii) Relative mode (iv) Auto increment mode. (08 Marks)
- b. Explain shift and rotate operations with examples. (08 Marks)
- c. Explain Big-Endian and Little-Endian method of byte addressing with an example. (04 Marks)

Module-2

- 3 a. Explain the working of the Direct Memory Access (DMA) controller in detail. Also, with the supporting diagram, explain different registers in a DMA interface. (08 Marks)
- b. Explain centralized and distributed BUS Arbitration, with diagrams. (08 Marks)
- c. Explain how interrupt requests from several input/output devices can be communicated to a processor using Daisy Chain Mechanism. (04 Marks)

OR

- 4 a. Using the Timing diagram of an input Data Transfer and the Handshake scheme, explain the input operation on an asynchronous BUS. (08 Marks)
- b. Draw the block diagram of universal serial BUS structure connected to the host computer. Briefly explain all fields of packets that are used for communication between a host and a device connected to a USB port. (08 Marks)
- c. Explain with a block diagram the keyboard to processor connection in parallel port. (04 Marks)

Module-3

- 5 a. Draw the organization of a 1K x 1 memory cell and explain it's working. (06 Marks)
- b. Explain the internal organization of a 16-Megabit dynamic RAM (DRAM) chip configured as 2M x 8 cells, with a neat diagram. (08 Marks)
- c. Assume a disk unit has 24 recording surfaces. It has a total of 14,000 cylinders. There is an average of 400 sectors per track. Each sector contains 512 bytes of data.
 - (i) What is the maximum number of bytes that can be stored in this unit?
 - (ii) What is the data transfer rate in bytes per second at a rotational speed of 7200 rpm?
 - (iii) Using a 32-bit word, suggest a suitable scheme for specifying the disk address, assuming that there are 512 bytes per sector. (06 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. 2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

OR

- 6 a. With a block diagram, explain the direct and set associative mapping between cache and main memory. (08 Marks)
- b. Draw a neat diagram of memory hierarchy in contemporary computer system. Also indicate relative variation of size, speed and cost per bit in the hierarchy. (06 Marks)
- c. Explain with a block diagram, how the translation look aside buffer is used in implementing virtual memory. (06 Marks)

Module-4

- 7 a. Explain the design of a four-bit carry look ahead adder. (06 Marks)
- b. Explain Booth's algorithm. Multiply using Booth's multiplication for the given Multiplicand : 0 1 0 1 1 0 1 and Multiplier : 0 0 1 1 1 1 0. (06 Marks)
- c. Design sequential circuit binary multiplier with a neat block diagram. Realize the above circuit for binary multiplier to calculate $+13 \times +11$. (08 Marks)

OR

- 8 a. Solve using restoring division for the given Dividend : 1000 and Divisor : 00011. Also, write the algorithm steps. (08 Marks)
- b. Using carry-save addition of Summands (CSA) for 4-bit operands. Perform multiplication between 45 and 63. (08 Marks)
- c. Show and explain the IEEE floating point representation for 32-bit (single precision) number. (04 Marks)

Module-5

- 9 a. Analyze the single bus architecture with a neat diagram and write the sequence of control steps to execute the instruction ADD R₁, R₂, R₃. (08 Marks)
- b. Analyze the multiple bus architecture with a neat diagram and write the sequence of control steps to execute the instruction ADD R₁, R₂, R₃. (08 Marks)
- c. List the remote functionality of home telemetry system. (04 Marks)

OR

- 10 a. Discuss the following in detail:
 (i) NUMA processor (08 Marks)
 (ii) UMA processor. (08 Marks)
- b. With a neat diagram, explain the working of a digital camera. (08 Marks)
- c. Compare Hardwired control unit with micro-programmed control unit. (04 Marks)
