CBCS SCHEME

USN | | | | | | | | | | |

18MT36

Third Semester B.E. Degree Examination, Feb./Mar.2022
Computer Organization & Architecture

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. With neat diagram, explain connection between the processor and the memory. **(10 Marks)**

b. What is straight line sequencing? Write a straight line program segment that appears in memory for adding 'n' numbers. **(10 Marks)**

OR

2 a. Explain Little endian and Big endian assignment with neat diagram and example. **(10 Marks)**

b. What is a bus? Explain the advantages and disadvantages of single bus structure with a neat diagram? Write a basic performance equation. **(10 Marks)**

Module-2

3 a. Define addressing mode. Explain 4 addressing mode with example. **(10 Marks)**

b. Explain the assembler directive concept with a neat diagram. **(10 Marks)**

OR

4 a. Define stack. Explain push and pop operation with instructions. **(10 Marks)**

b. What is subroutine linkage? With example explain different ways of passing parameters to subroutines. **(10 Marks)**

Module-3

5 a. Define interrupt. Discuss the different schemes available to enable and disable interrupts. **(10 Marks)**

b. What is interrupt nesting? Explain with a neat diagram the implementation of interrupt priority using individual interrupt request and acknowledge lines. **(10 Marks)**

OR

6 a. What is DMA? With a neat diagram, discuss how DMA controller registers accessed by the processor to initiate transfer operations? **(10 Marks)**

b. Explain how simultaneous interrupt requests from several I/O devices will be handled by a processor using daisy chain arrangement. **(10 Marks)**

Module-4

7 a. Draw the organization of 1 K×1 memory chip and explain its working. **(10 Marks)**

b. Define ROM. Explain the single ROM cell and list and explain various types of ROMs. **(10 Marks)**

OR

8 a. Draw the organization of 2M×8 dynamic memory chip and explain its working. **(10 Marks)**

b. Explain synchronous DRAMs along with burst read of length 4 in a SDRAM. **(10 Marks)**

Module-5

9 a. With a neat diagram, explain single bus organization of the data path inside a processor. **(10 Marks)**

b. Explain the hard wired control unit organization in a processing unit. **(10 Marks)**

OR

10 a. Write a control sequence for the execution of the instruction add R_4, R_5, R_6 in three bus organizations. **(10 Marks)**

b. Explain the microprogrammed control unit organization in a processing unit. **(10 Marks)**

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