# CBCS SCHEME

18ELN14/24

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## First/Second Semester B.E. Degree Examination, July/August 2021
## Basic Electronics

Time: 3 hrs.                                                                    Max. Marks:100

### Note: Answer any FIVE full questions.

1  a. Explain the operation of p–n junction Diode under unbiased condition with a neat diagram. **(08 Marks)**

   b. In a full wave rectifier, input is from 30 – 0 – 30V. The load and $R_f$ are 100Ω and 10Ω respectively. Calculate area voltage, efficiency, percentage regulation. **(06 Marks)**

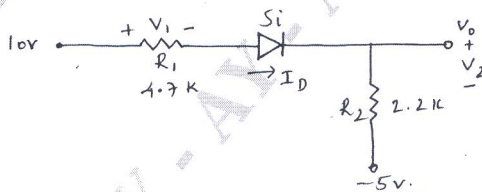   c. Determine $I_D$, $V_1$, $V_2$ and $V_0$ for the given circuit.



Fig.Q1(c)                                                                       **(06 Marks)**

2  a. With a neat diagram and waveforms explain the working of a bridge rectifier. **(08 Marks)**

   b. Explain the operation of a zener diode with line regulation and load regulation. **(08 Marks)**

   c. For a zener regulator shown in Fig.Q2(c), calculate the range of input voltage for which output remain constant. $V_Z = 6.1V$, $I_{Zmin} = 2.5mA$, $I_{Zmax} = 25mA$, $r_Z = 0Ω$.
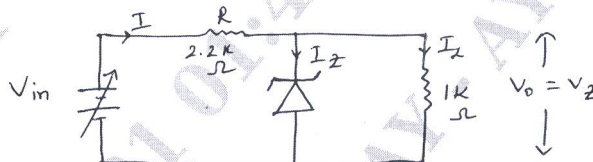


Fig.Q2(c)                                                                       **(04 Marks)**

3  a. Explain the characteristics of N-channel JFET(Drawn and transfer characteristics). **(12 Marks)**

   b. For a N-channel JFET, $I_{DSS} = 8mA$, $V_P = -5V$. Find :
      i) $I_D$ @ $V_{GS} = -2V$ and $-3V$
      ii) $V_{GS}$ @ $I_D = 3mA$ and $5mA$. **(06 Marks)**

   c. List out classification of FET with symbols. **(02 Marks)**

4  a. Draw and explain forward and reverse characteristics of an SCR. **(07 Marks)**

   b. Sketch the transfer and drain characteristics for an n-channel depletion – type MOSFET for the range of values of $V_{GS} = -6V$ to $+1V$ with $I_{DSS} = 8mA$, $V_P = V_{GS(off)} = -6V$. **(08 Marks)**

   c. With a neat diagram, explain the 2 transistor model of SCR. **(05 Marks)**

5  a. Explain following with respect to OP-Amp.
      i) Virtual ground        ii) CMRR             iii) Slew rate
      iv) Offset voltage       v) Matched transistors. **(10 Marks)**

   b. Derive the expression for output voltage of an
      i) integrator    ii) inverting summing amplifier. With a neat circuit diagram. **(10 Marks)**

6    a.   Explain the ideal characteristics of on op-Amp.      (08 Marks)

     b.   Derive the expression for output voltage of an non inventing amplifier with a neat circuit and waveform.      (08 Marks)

     c.   Design an adder circuit using an op-Amp to obtain output expression.
$V_0 = -2(0.1V_1 + 0.5V_2 + 20V_3)$.      (04 Marks)

7    a.   Explain the operation of BJT as an amplifier and as a switch.      (10 Marks)

     b.   Draw and explain the operation of a voltage series −ve feedback amplifier and derive an expression for its input impedance.      (10 Marks)

8    a.   Define an oscillator. Explain Brakhausen's criteria for oscillations with block diagram.      (06 Marks)

     b.   Derive the expression for frequency of oscillations of Wien bridge oscillator.      (08 Marks)

     c.   With a neat diagram, explain the working of RC phase shift oscillator.      (06 Marks)

9    a.   Subtract $(111001)_2$ from $(101011)_2$ using 2's complement method.      (04 Marks)

     b.   State and prove Demorgan's theorem for 3 variables.      (04 Marks)

     c.   Simplify the following Boolean expression :

        i)    $A + \overline{A}B = A + B$

        ii)   $\overline{\overline{X}\overline{Y}\overline{Z}} + \overline{\overline{X}Y\overline{Z}} + \overline{X}\overline{Y} + X\overline{Y}$

        iii)   $\overline{\overline{\overline{XY + XYZ}} + X(Y + X\overline{Y})}$

        iv)   $ABC + A\overline{B}C + AB\overline{C} + \overline{A}BC$

        v)   $\overline{\overline{\overline{A\overline{B} + ABC}} + A(B + A\overline{B})}$

        vi)   $AB + \overline{AC} + A\overline{B}\,C(AB + C)$.      (12 Marks)

10   a.   With block diagram and truth table, explain the operation of full ladder using 2 half adder.      (08 Marks)

     b.   Explain the operation NOT, AND and OR gates using analogous switch equivalent circuit.      (09 Marks)

     c.   Implement Ex – OR gate using only NOR gate.      (03 Marks)

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