

Third Semester B.E. Degree Examination, July/August 2022 Electronic Devices

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. In a filled band, what is the net current density and if a hole is created, what is the net current generated? Describe the superposition of the (E,K) band structure for a semiconductor in an electric field. (10 Marks)
- b. A Si bar 4 cm long and $500 \mu\text{m}^2$ in cross sectional area is doped with $2.5 \times 10^{18} / \text{cm}^3$ phosphorus. Find the current at 300°K with 22 V applied voltage. How long it take an average electron to drift 4 cm in pure silicon at an electric field of 70 V/cm. Calculate the time required at 10^5 V/cm. Assume mobility of the electrons is $0.1675 \text{ m}^2/\text{Vsec}$ and scattering limited velocity (V_s) in 10^7 cm/sec. (10 Marks)

OR

- 2 a. Show the random thermal motion of an electron in a solid and what happens when electric field is applied? Derive the equation which relates the current density and mobility in a semiconductor in an applied electric field. (10 Marks)
- b. Consider a semiconductor bar with width = 0.02 cm, thickness = $15 \mu\text{m}$ and length = 8 mm. For $B_z = 15 \text{ kg}$ and a current of 3.5 mA, $V_{AB} = -5 \text{ V}$, $V_{CD} = 400 \text{ mV}$, find the type, concentration and mobility of the majority carrier. (10 Marks)

Module-2

- 3 a. Analyze the effect of a bias at a pn junction on electric field, potential particle flow and current direction at (i) Equilibrium (ii) Forward bias (iii) Reverse bias. (12 Marks)
- b. Explain the operation of pin photodetector. (08 Marks)

OR

- 4 a. What type of breakdown occurs in a lightly doped pn junction? Show the energy band diagram of a pn junction in a reverse bias, single ionizing collision by an incoming electron in the depletion region and primary, secondary and tertiary collisions. (10 Marks)
- b. Obtain the relationship between the open circuit voltage and optical generation rate starting from the expression for the optically generated illuminated pn junction. (10 Marks)

Module-3

- 5 a. Derive the Ebers-Moll equations for the thermal currents in a transistor and represent the same. (14 Marks)
- b. When the base narrowing effect occur in a transistor? (06 Marks)

OR

- 6 a. Illustrate the hole and electron flow in a pnp transistor with proper biasing. (10 Marks)
- b. Show the switching effects in a common emitter transistor circuit. (10 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
 2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-4

- 7 a. Show the electric field direction, charge flow and induced charge region in a MOS capacitor with P-type substrate and n-type substrate when a moderate positive gate bias is applied. (08 Marks)
- b. Represent the energy-band diagram through a MOS capacitor structure with P-type as a semiconductor and differential charge distribution for a differential change in gate voltage in the depletion and inversion mode. (12 Marks)

OR

- 8 a. Represent the energy band diagram of a MOS capacitor for the following cases :
 (i) Negative gate bias in a MOS capacitor with ptype substrate.
 (ii) Positive gate bias in a MOS capacitor with ntype as substrate. (10 Marks)
 (iii) Large negatve gate bias in a MOS capacitor with n type as substrate. (10 Marks)
- b. Show the channel formation in the MOS structure and I_D versus V_{DS} curve for the following cases :
 (i) $V_{gs} > V_t$ and small V_{DS} value.
 (ii) $V_{gs} > V_t$ and large V_{DS} value.
 (iii) $V_{gs} > V_t$ and $V_{DS} = V_{DS}(\text{sat})$. (10 Marks)

Module-5

- 9 a. Write the names of the different fabrication steps in a pn junction. (08 Marks)
 b. Explain the evolution of ICs over the years. (12 Marks)

OR

- 10 a. Draw a neat sketch showing the ion implantation system in the fabrication of a pn junction and explain. (10 Marks)
 b. Write the structure of a CMOS inverter and show the formation of p-channel and n-channel devices together. (10 Marks)
