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10EC45

Fourth Semester B.E. Degree Examination, July/August 2022
Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

PART – A

1 a. Explain Verilog Data types. **(06 Marks)**
b. Write Shift and Rotate Operators used in VHDL. **(04 Marks)**
c. What are different styles of description used in HDL? Explain any two of them by taking examples. **(10 Marks)**

2 a. Write VHDL code for 2 × 1 multiplexer with active low enable in dataflow descriptions, with neat sketches. **(08 Marks)**
b. Design 2 × 2 Magnitude Comparator and write VHDL/Verilog Code for the same. **(09 Marks)**
c. Explain the Execution of Signal Assignment Statements. **(03 Marks)**

3 a. Explain the flow chart of Booth Multiplier Algorithm with example. Write VHDL Code for 4 × 4 Booth Algorithm. **(12 Marks)**
b. Write down the behavioural description of D – Latch using variable assignment statements with waveforms in Both VHDL and Verilog. **(08 Marks)**

4 a. Write the VHDL structural description of full adder using two half adders and an OR gate. Write simulation waveform. **(10 Marks)**
b. What is Binding in VHDL? Explain i) Binding between entity and architecture in VHDL.
ii) Binding between two modules in Verilog.
iii) Binding between library and module in VHDL. **(10 Marks)**

PART – B

5 a. What are the significance of Procedure , Task and Function? Differentiate between Procedure / Task and function. **(06 Marks)**
b. Write HDL Code for converting an unsigned binary to an integer using Procedure and Task. **(08 Marks)**
c. Write a Verilog function to find greater of two numbers. **(06 Marks)**

6 a. Discuss VHDL packages with example. **(04 Marks)**
b. Draw the block diagram and function table and write the verilog description for 16 × 8 SRAM. **(12 Marks)**
c. Discuss the importance of mixed type description. **(04 Marks)**

7 a. How to invoke Verilog module from VHDL module? Explain with an example of a mixed language description for a full adder using 2 half adders. **(10 Marks)**
b. Write Mixed – Language description of a JK FlipFlop with a clear input and draw simulation waveforms. **(10 Marks)**

8 a. Discuss Synthesis. List steps involved in synthesis with flow chart. **(10 Marks)**
b. Write a behavioral code in VHDL and Verilog for signal assignment statement Y – X. Explain the mapping to gate level logic diagram. **(06 Marks)**
c. Discuss Synthesis information extraction from entity in VHDL. **(04 Marks)**

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