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10EC56

Fifth Semester B.E. Degree Examination, July/August 2022
Fundamentals of CMOS VLSI

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO full questions from each part.***

PART – A

1 a. Explain how the CMOS inverter can act as an amplifier. Describe the function of CMOS differential inverter and discuss the different types of differential amplifiers. **(07 Marks)**

b. Obtain the size of the transistor for a CMOS circuit of 250nm technology has its noise margin V_{NML} = 0.5V, low input voltage is 0.26V. Assume V_{DD} = 5V, V_{TN} = 0.7V, V_{TP} = -0.8V, $K_n = 150\mu A/v^2$, $K_p = 68\mu A/v^2$, $w_n = 0.5\mu m$.

$$\left(\text{Hint : } V_{OL} = (V_{DD} - V_{Tn}) - \sqrt{(V_{DD} - V_T)^2 - \frac{\beta_p}{\beta_n}(V_{DD} - V_{Tp})^2}\right).$$ **(07 Marks)**

c. Explain the steps involved in n-MOS fabrication with neat diagram and list out the required number of masks. **(06 Marks)**

2 a. What do you understand about λ-based rules? Draw the schematic and layout for the tristate inverter and mark the width of each layer as per lambda based rule. **(08 Marks)**

b. Discuss the effect of channel length modulation on the performance of nMOS transistor. **(04 Marks)**

c. Calculate the delay of the given layer. In 5μm technology consider the sheet resistance of metal is 0.03Ω, sheet resistance of polysilicon is 25Ω and for n-diffusion is $10^4\Omega$. Similarly the relative capacitance for metal is 0.075□C_g, for poly 0.1□C_g and for diffusion is 0.25□C_g. **(08 Marks)**

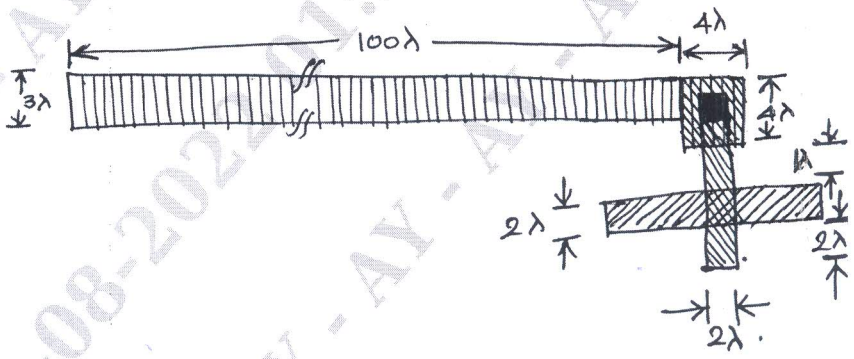

Fig.Q.2(c)

3 a. Design a n-MOS pass transistor logic circuit for the sum function of full adder circuit. Show the design with neat steps. **(07 Marks)**

b. Draw and explain the circuit of BICMOS inverter and highlight the need for BICMOS technology. **(07 Marks)**

c. Draw the dynamic CMOS logic circuit for the XNOR gate and show clearly how it works as a XNOR gate. **(06 Marks)**

4 a. Draw the rise time and fall time model for 1:1 CMOS inverter and obtain the expression for both rise time and fall time. **(06 Marks)**

b. Scale the below given device parameters:
   i) Gate Area (A_g)
   ii) Gate capacitance (C_g)
   iii) Carrier density in channel
   iv) Channel resistance
   v) Maximum operating frequency (f_o)
   vi) Current density (J). **(06 Marks)**

c. Discuss the limitations of scaling. **(08 Marks)**

PART – B

5 a. Design the 6-bit structured arbitration logic. Explain the working principle of your design with its circuit diagram and truth table, and also draw the stick diagram for the single structured cell. **(08 Marks)**

b. What do you understand about PLA? Draw the PLA logic circuit for the given expression.

$Z_1 = a\bar{b}\bar{d}e + \bar{a}\bar{b}\bar{c}\bar{e} + bc + de$

$Z_2 = \bar{a}\bar{c}e + ce$

$Z_3 = bc + de + \bar{c}\bar{d}\bar{e} + bd$. **(05 Marks)**

c. Draw the 3-bit dynamic shift register and explain it briefly. **(07 Marks)**

6 a. Explain the 12-bit carry skip adder with its architecture for 4 bits in a group and show the πP_i and carry values to add the given numbers. Explain its skipping technique.
A = 0010 1011 1000, B = 1100 0000 0111. **(10 Marks)**

b. Explain the arrangement of 4-bit serial parallel multiplier with its block diagram and working principle. **(10 Marks)**

7 a. Explain the pseudo static RAM/register cell with its neat diagram. **(07 Marks)**

b. Explain the 3-T dynamic RAM cell with neat sketch. Calculate the number of bits that can be stored in the chip area of 6mm × 6mm, if the 3T-RAM stores a single bit in the area of $500\lambda^2$ in 2.5μm technology. **(07 Marks)**

c. Explain the pseudo static D-flipflop with neat sketch and define the setup time and holdtime of D-flipflop. **(06 Marks)**

8 a. Define observability and controllability. **(04 Marks)**

b. Define stuck-at fault model of digital logic circuits. **(04 Marks)**

c. What do you understand about D-algorithm? Explain the algorithm by generating atleast one vector for the specified fault in the given circuit. **(12 Marks)**

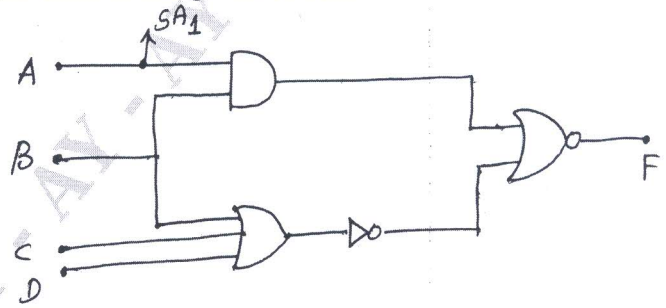

Fig.Q.8(c)

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