CBCS SCHEME

USN | | | | | | | | | | |

15EE35

Third Semester B.E. Degree Examination, July/August 2022
Digital System Design

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define combinational logic. List out the various steps in designing a combinational logic circuit. **(04 Marks)**

b. Distinguish prime implicante and essential prime implicante. Determine the same of the function using K –maps $f(w, x, y, z) = \Sigma m(0, 2, 5, 7, 8, 10, 13, 15)$. Hence the minimal sum expression. **(08 Marks)**

c. Design a logic circuit with inputs A, B and C so that output Y is high, whenever A is zero or whenever B = C = 1 using only two input NAND gates. **(04 Marks)**

OR

2 a. Obtain minimal product of the Boolean function using VEM technique
$X = f(a, b, c) = \Sigma_m(0, 1, 4, 5, 7)$. **(04 Marks)**

b. Simplify the function using K – maps
$T = f(a, b, c, d) = \Sigma_m(1, 3, 4, 5, 13, 15) + \Sigma_d(8, 9, 10, 11)$. **(04 Marks)**

c. Simplify the function using Quine McCluskey techniques and realize the simplified function using NOR gates
$f(a, b, c, d) = \Sigma_m = (7, 9, 12, 13, 14, 15) + \Sigma_d(4, 11)$. **(08 Marks)**

Module-2

3 a. Design a combinational circuit to convert BCD number to Excess–3 BCD number as following :
i) Construct the truth table
ii) Simplify each output function and write the reduced equation
iii) Draw a logic diagram. **(10 Marks)**

b. Design a 4 to 16 line decoder using 2 to 4 line decoder with active low enable and active low outputs. **(06 Marks)**

OR

4 a. Design a binary full adder using minimum member of NAND gates. Write it truth tables. **(06 Marks)**

b. What is lookahead carry adder? Derive an expression for C_{out} for a four stage lookahead carry adder. **(06 Marks)**

c. Implement the Boolean function using 4: 1 multiplexer
$Y = f(x, y, z) = \Sigma_m(1, 3, 5, 6)$. **(04 Marks)**

Module-3

5 a. Differentiate sequential logic circuit and the combinational logic circuit. **(04 Marks)**

b. Explain with timing diagram, the working operation of SR Latch as a switch debouncer. **(06 Marks)**

c. Obtain the characteristic equation of JK and D flipflops. **(06 Marks)**

OR

6 a. With the help of logic diagram, explain the following with respect to the shift register
i) Parallel in and serial out
ii) Ring counter and twisted ring counter. **(08 Marks)**

b. Design of a synchronous Mod – 6 counter using D – flipflops to count that sequence 0, 2, 3, 6, 5, 1, 0, . . used as state diagram. **(08 Marks)**

Module-4

7 a. With a suitable block diagram, explain the Mealy and Moore model, in a sequential circuit analysis. **(06 Marks)**

b. Analysis the following sequential circuit shown in Fig.Q7(b) and obtain
i) FlipFlop input and output equation
ii) Transition equation and table
iii) State stable
iv) Draw a state diagram.

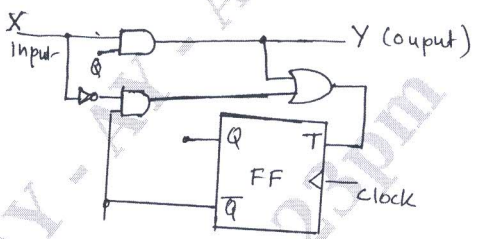

Fig.Q7(b) **(10 Marks)**

OR

8 a. Write a note on construction of the state diagram with sequence detector. **(08 Marks)**

b. Draw the state diagram of Mealy machine whose output is 1, if the last three inputs were 010 assuming that the sequence could overlap. **(08 Marks)**

Module-5

9 a. Explain the structure of the VHDL modules with an examples. **(06 Marks)**

b. Compare VHDL module and verilog module. **(04 Marks)**

c. Mention the types of HDL description. Explain how a half adder can be modeled in VHDL in any one of the description method. **(06 Marks)**

OR

10 a. Explain the execution of signal assignment statements in HDL. **(06 Marks)**

b. List the data types used in VHDL and Verilog. **(04 Marks)**

c. Write verilog code for 2 × 1 multiplexer with an active low enable inputs. **(06 Marks)**

* * * * *