CBCS SCHEME

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15EE34

Third Semester B.E. Degree Examination, July/August 2022
Analog Electronic Circuits

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain the fixed bias circuit with load lien analysis. **(08 Marks)**

b. Write the procedure for analyzing the clamper circuit. Determine the output voltage for the network shown in Fig.Q1(b). Assume f = 1KHz and ideal diode.

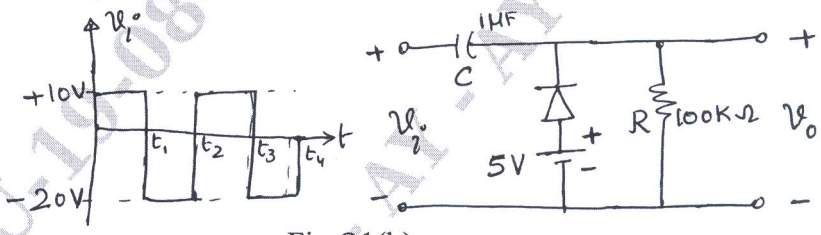

Fig.Q1(b) **(08 Marks)**

OR

2 a. Explain the operation of transistor as switch along with suitable circuit and necessary waveforms. **(08 Marks)**

b. For the circuit shown in Fig.Q2(b), I_C = 2mA, β = 100. Calculate R_E, V_{CE} and S_{ICO}. Assume S_i transistor.

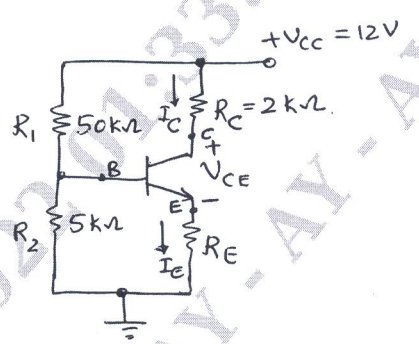

Fig.Q2(b) **(08 Marks)**

Module-2

3 a. Derive the expressions for A_i, A_v, R_i and R_0 for CE amplifier using h – parameter model. **(08 Marks)**

b. For the emitter follower circuit shown in Fig.Q3(b). Calculate Z_i, Z_0, A_v and A_i.
Take : h_{ie} = 1.1KΩ ; $h_{re} = 2.5 \times 10^{-4}$; h_{fe} = 50 ; h_{oe} = 24μA/v.

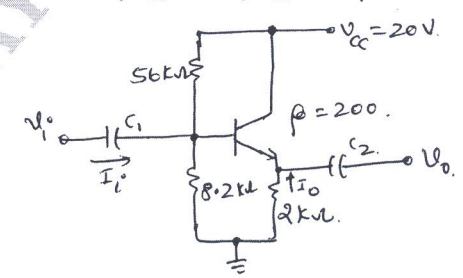

Fig.Q3(b) **(08 Marks)**

OR

4 a. Starting from fundamentals, define h – parameters and obtain are h – parameter equivalent circuit of common emitter configuration. **(08 Marks)**

b. Prove that Miller effect input capacitance, $C_{ni} = (1 - A_v)C_f$ and output capacitance, $C_{M0} = \left(1 - \frac{1}{A_v}\right)C_f$, where A_v and C_f have their usual meanings. **(08 Marks)**

Module-3

5 a. Derive the expression for input and output impedances for feedback amplifier employing voltage series feedback. **(08 Marks)**

b. Obtain an expression for voltage gain, input impedance and output impedance of a Darlington emitter follower. **(08 Marks)**

OR

6 a. With block diagram, explain the concept of different types of feedback connection. **(08 Marks)**

b. If an amplifier has mid-based voltage gain of 1000 with $f_L = 50Hz$ and $f_H = 50KHz$, if 5% feedback is applied then calculate f_L and f_H with feedback. **(05 Marks)**

c. A given amplifier arrangement has the following voltage gains, $A_{v_1} = 10$, $A_{v_2} = 20$ and $A_{v_3} = 40$. Calculate the overall voltage gain in dB. **(03 Marks)**

Module-4

7 a. Explain the operation of class B push – pull amplifier and derive its conversion efficiency. **(10 Marks)**

b. The following distortion reading are available for a power amplifier : $D_2 = 0.2$, $D_3 = 0.02$, $D_4 = 0.06$ with $I_1 = 3.3A$ and $R_C = 4\Omega$. Calculate THD, fundamental power component and total power. **(06 Marks)**

OR

8 a. Obtain an expression for frequency of oscillation in Colpitt's oscillator. **(10 Marks)**

b. With circuit diagram, explain the working principle of crystal oscillator in series resonant mode. **(06 Marks)**

Module-5

9 a. With the help of neat diagram, explain the construction, working of characteristics of n – channel JFET. **(10 Marks)**

b. For the circuit shown in Fig.Q9(b). Calculate : I_D, V_{GS}, V_G, V_{DS} and V_S.

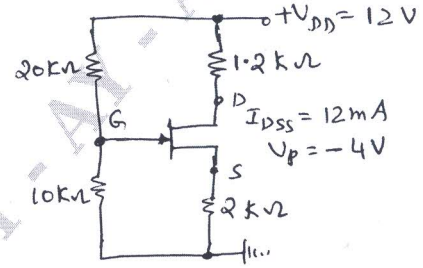

Fig.Q9(b) **(06 Marks)**

OR

10 a. With the help of neat diagrams, explain the construction, working and characteristics of n-channel DMOSFET. **(10 Marks)**

b. Differentiate between BJT and FET. **(06 Marks)**

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