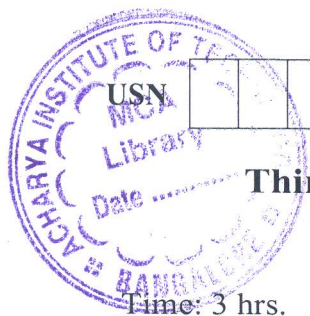


CBCS SCHEME

17MT35



Third Semester B.E. Degree Examination, July/August 2022 Analog and Digital Electronics

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Design a first order lowpass filter with cut off frequency of 1kHz with a passband gain of 2 plot the frequency response. (10 Marks)
- b. Explain the operation of second order highpass filter with neat circuit diagram and waveform. (10 Marks)

OR

- 2 a. Explain the operation of notch filter with neat circuit diagram and frequency response. (10 Marks)
- b. With neat circuit diagram, explain the working of all pass filter and derive the expression for voltage gain and phase angle. (10 Marks)

Module-2

- 3 a. With neat circuit diagram explain the operation of phase shift oscillator and derive the expression for frequency of oscillations. (10 Marks)
- b. Explain the operation of wien bridge oscillator. (10 Marks)

OR

- 4 a. Explain the operation of non inverting and inverting comparator with circuit diagrams and wave forms. (10 Marks)
- b. Explain the operation of Schmitt trigger with the help of circuit diagram, waveform and Hysterisis curve. (10 Marks)

Module-3

- 5 a. Explain the operation of 555 timer using the internal architecture. (10 Marks)
- b. Explain the working of 555 timer as a monostable multivibrator. (10 Marks)

OR

- 6 a. Explain the operation of 555 timer as a astable multivibrator. (10 Marks)
- b. Explain any two applications of astable multivibrator. (10 Marks)

Module-4

- 7 a. Simplify the following Boolean equations using K-maps:
 - i) $F(ABCD) = A'B'C' + B'CD' + A'BCD' + AB'C'$
 - ii) $F(w, x, y, z) = \sum (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$. (10 Marks)
- b. Explain the full adder and full subtractor with truth table and logic diagram using gates. (10 Marks)

OR

- 8 a. Implement the following function with a multiplexer $F(ABCD) = \Sigma(0, 1, 3, 4, 8, 9, 15)$. (10 Marks)
- b. Design a BCD to decimal decoder draw the truth table and logic diagram. (10 Marks)

Module-5

- 9 a. Explain the operation clocked RS flipflop and D-flipflop using timing diagram and truth table. (10 Marks)
- b. Explain the JK master slave flip flop with schematic diagram, timing diagram and truth table. (10 Marks)

OR

- 10 a. Explain the working of modulo 16 ripple up counter with schematic, timing and state diagram. (10 Marks)
- b. Explain a 3-bit synchronous counter with schematic and truth table. (10 Marks)
