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10CS74

Seventh Semester B.E. Degree Examination, Jan./Feb. 2023
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Find the Good number of dies per 30 cm Wofer for a die that is
i) 1.5 cm on a side
ii) 1.0 cm on a side
Assume defect density is 4.0 per cm^2 and α is 4. **(10 Marks)**

b. Define Amdhol's law. Derive expression for CPU clock or a function of instruction count clocks per instruction and clock cycle time. **(10 Marks)**

2 a. What are major hazards in a pipe line? What are methods to minimize data hazard explain with example. **(10 Marks)**

b. With diagram implement Basic Pipe Line for MIPS. **(10 Marks)**

3 a. Show that the number of effective clock cycles required for loop unrolling in 3.5 clock cycles. Given

```
for (i = 1000 ; i > 0 ; i = i - 1)
    x[ i ] = x [ i ] + s ;
```

Assume the latency

Inst. Producing Result	Inst. Using Result	Latency in Clk Cy
FP ALU op	FP ALU op	3
FP ALU op	Store double	2
Load double	FP ALU op	1
Load double	Store double	0

(10 Marks)

b. Implement Hardware – Based speculation. **(10 Marks)**

4 a. Explain the Basic VLIW approach for exploiting ILP using multiple issues. **(10 Marks)**

b. What are the key issues in implementing advanced speculation techniques? Explain in detail. **(10 Marks)**

PART – B

5 a. Explain Flynn proposed model of categorizing computers. **(05 Marks)**

b. Implement snooping protocols for shared memory multiprocessor. **(10 Marks)**

c. Write short notes on synchronization. **(05 Marks)**

6 a. Along with diagram explain organization of data cache in AMD Multiprocessor (Opteron). **(05 Marks)**

b. Which has lower miss rate: 16 KB instruction cache with 16 KB data cache or 32 KB unified cache. Assume
Miss rate of 16 KB Instruction cache = 3.82
Miss rate of 16 KB Data cache = 40.9
Miss rate of 32 KB Unified = 43.3
36% of instructions are data transfer instruction Hit Rate 1 clock cycle, Miss penalty 100 clock cycles. What is average memory access time? **(10 Marks)**

c. Explain Six Basic optimizations. **(05 Marks)**

7 a. Explain various advanced optimization steps for
(i) Reduced the Hit time
(ii) Increase cache bandwidth. **(06 Marks)**
b. Explain compiler optimizations to reduce Miss Rate. **(08 Marks)**
c. Explain the protection of Virtual Machines. **(06 Marks)**

8 a. Explain in detail, the hardware support for preserving exception behavior during speculation. **(10 Marks)**
b. Explain the prediction and speculation support provided in IA64. **(10 Marks)**

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