CBCS SCHEME

USN | | | | | | | | | | |

18EC35

Third Semester B.E. Degree Examination, June/July 2023
Computer Organization and Architecture

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Explain with a neat diagram, the basic Operational concept of a Computer. **(08 Marks)**
b. Explain how to measure the performance of a Computer. **(06 Marks)**
c. Write a note on Types of Computers. **(06 Marks)**

OR

2 a. Explain IEEE standard for Floating point number. **(08 Marks)**
b. Explain the methods to improve the performance of Computer. **(08 Marks)**
c. Write a note on Processor clock. **(04 Marks)**

Module-2

3 a. What is an Addressing Mode? Explain any four addressing mode with an example. **(10 Marks)**
b. With an example, explain the concept of BIG – ENDIAN and LITTLE – ENDIAN Assignment of Memory Storage. **(10 Marks)**

OR

4 a. Explain the concept of Stacks and Queues. **(08 Marks)**
b. What are Assembler directives? Explain the various assembler directives with examples. **(08 Marks)**
c. With an example, explain Shift and Rotate Instructions. **(04 Marks)**

Module-3

5 a. Define Interrupt. Explain Daisy chain and Priority Structure methods of handling interrupts from multiple devices. **(10 Marks)**
b. With a neat diagram, explain DMA Controller Operation with its Interface Registers. **(10 Marks)**

OR

6 a. Define Exceptions. Explain the different types of Exceptions. **(06 Marks)**
b. Explain the Tree structure of USB with Split bus operation. **(06 Marks)**
c. With a neat diagram, explain Centralized and distributed bus arbitration schemes. **(08 Marks)**

Module-4

7 a. Define Cache Memory. Explain various types with neat diagram. **(08 Marks)**
b. Write a note on Classification of a Memory Structure. **(04 Marks)**
c. Define the following terms :
i) Memory Latency ii) Memory Bandwidth
iii) Memory Access time iv) Memory Cycle time. **(08 Marks)**

OR

8 a. Explain with block diagram, the Operation of SD RAM. **(10 Marks)**

b. Define ROM Point out and explain various types of ROM's. **(10 Marks)**

Module-5

9 a. Explain with neat diagram, Single Bus Organisation of data path inside a processor. **(10 Marks)**

b. What are the actions required to execute a Complete Instruction Add(R3), R1? **(10 Marks)**

OR

10 a. Explain Hardwired Control Unit Organisation. **(10 Marks)**

b. Explain Multiple bus / three bus Organization, with a neat diagram. **(10 Marks)**

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