CBCS SCHEME

USN

17MT36

Third Semester B.E. Degree Examination, June/July 2023
Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain in brief the operational concept between processor and the memory. **(10 Marks)**
b. Explain (i) Basic performance equation (ii) Pipelining. **(10 Marks)**

OR

2 a. Write a note on Instruction and Instruction Sequencing. **(08 Marks)**
b. Explain Big Endian and Little Endian Byte and word addressing. **(04 Marks)**
c. Explain straight line program for adding n numbers. **(08 Marks)**

Module-2

3 a. Define addressing mode. Explain any three addressing mode with example. **(10 Marks)**
b. What is Stack? Write a routine for safe push and pop operation. **(05 Marks)**
c. Explain with example program how parameters are passed to subroutine using registers. **(05 Marks)**

OR

4 a. What is subroutine linkage method? Explain with example. **(06 Marks)**
b. Explain program controlled I/O operation with a neat diagram. **(06 Marks)**
c. What are assembler directives? Explain its use with assembly language program. **(08 Marks)**

Module-3

5 a. Write a note on :
(i) Interrupt hardware
(ii) Enabling and disabling of Interrupts **(10 Marks)**
b. Explain (i) Daisy chain (ii) Interrupt priority. **(10 Marks)**

OR

6 a. Write a brief note on Direct Memory Access along with control register. **(10 Marks)**
b. Write a note on parallel port interface between the keyboard to processor along with Input Interface circuit. **(10 Marks)**

Module-4

7 a. Explain the working of single transistor dynamic memory cell with a neat diagram. **(06 Marks)**
b. Explain the concept of memory interleaving with a neat diagram. **(06 Marks)**
c. What is ROM? Explain various types of ROM. **(08 Marks)**

OR

8 a. Explain the internal organization of 2m×8 dynamic memory chip with a neat diagram. **(06 Marks)**

b. What is virtual memory technique? Explain the organization of virtual memory with a neat diagram. **(06 Marks)**

c. Explain direct mapped cache and associative mapped cache with neat block diagram. **(08 Marks)**

Module-5

9 a. Write control sequence for execution of the instruction Add(R_3), R_1. **(10 Marks)**

b. Explain branching instruction concept with instruction. **(10 Marks)**

OR

10 a. Draw and explain multiple bus organization. **(10 Marks)**

b. With a neat block diagram, explain hardwired control unit show the generation Zin and End control signal. **(10 Marks)**

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